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PDN阻抗之抽丝剥茧

电源完整性之PDN

一博科技-SI研究部

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PART 01

电源噪声是怎么来的?

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一句话说明什么是：PI

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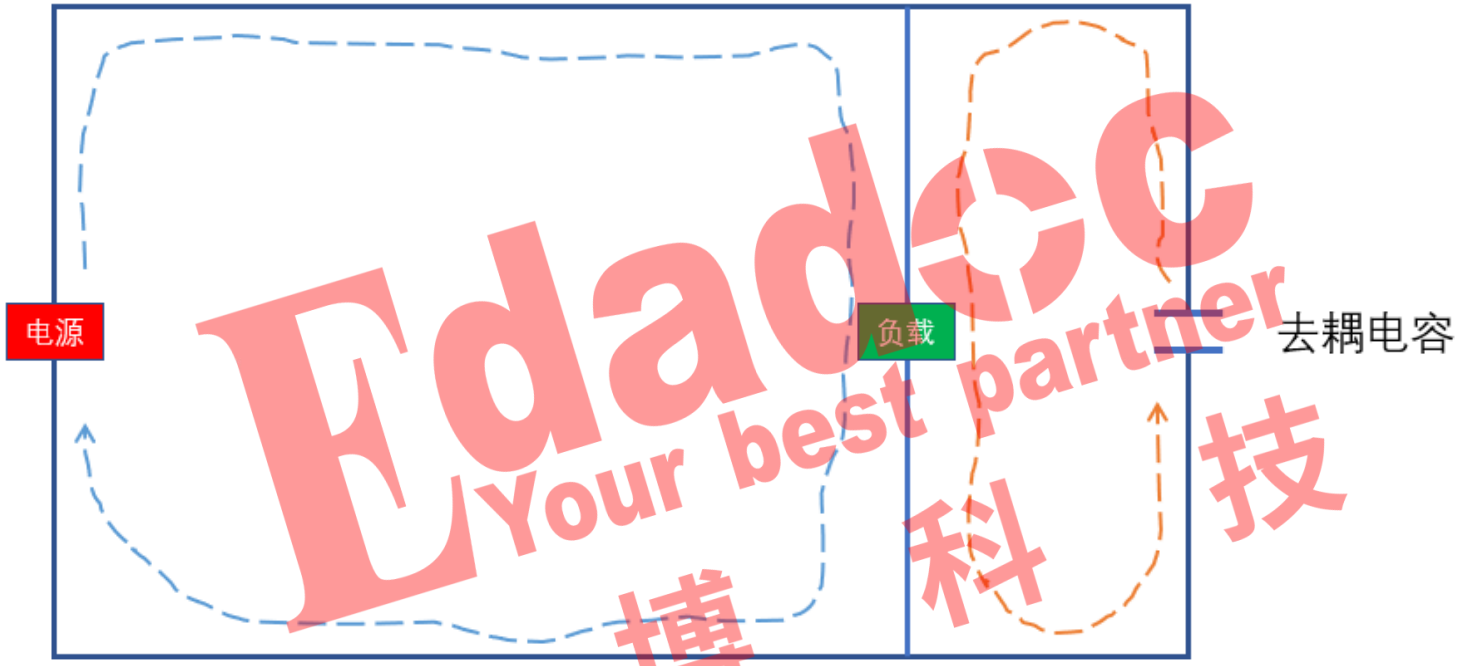
电源完整性最重要的参数

- 产生电源完整性问题的根本原因是什么?
- 哪一个参数决定了电源完整性设计的难度?



$$\Delta V = IR_{loop}(DC) + L_{loop}\frac{di}{dt}(AC)$$

直流IR Drop　交流 瞬态电压

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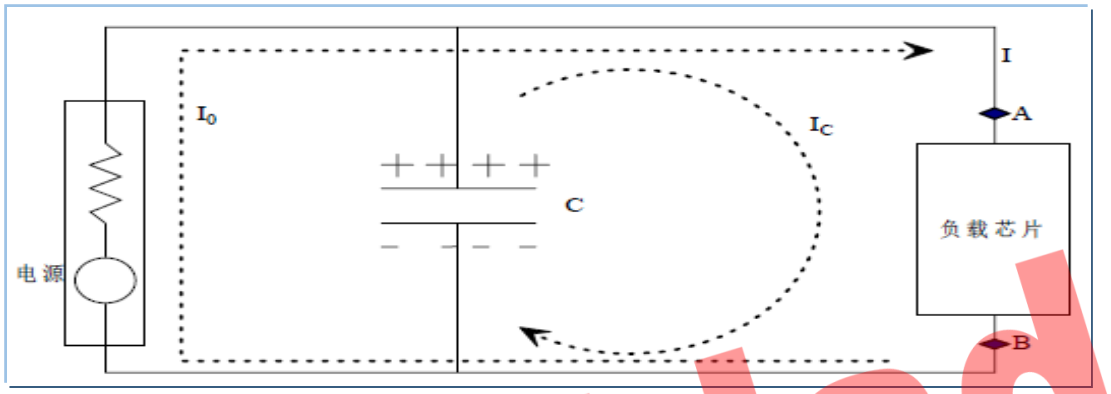
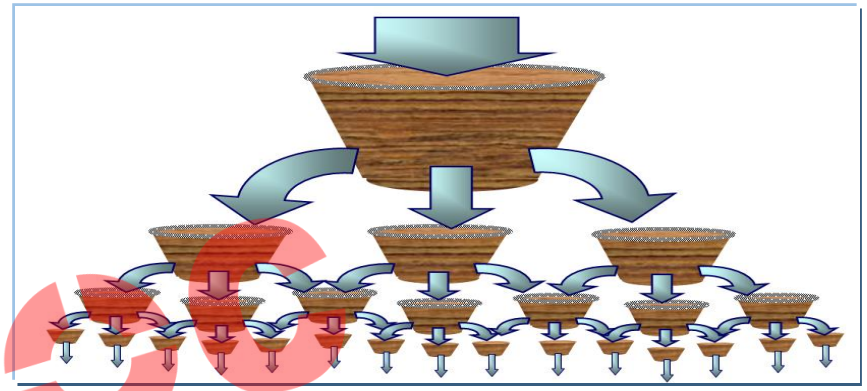
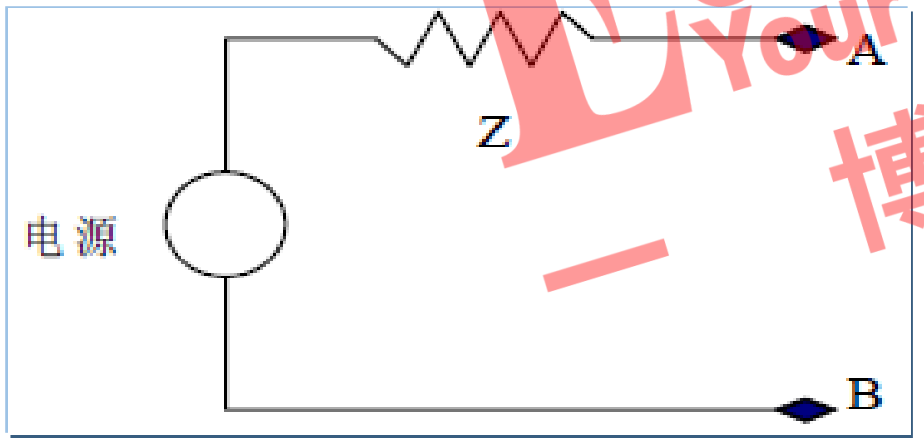
电源完整性分析方法

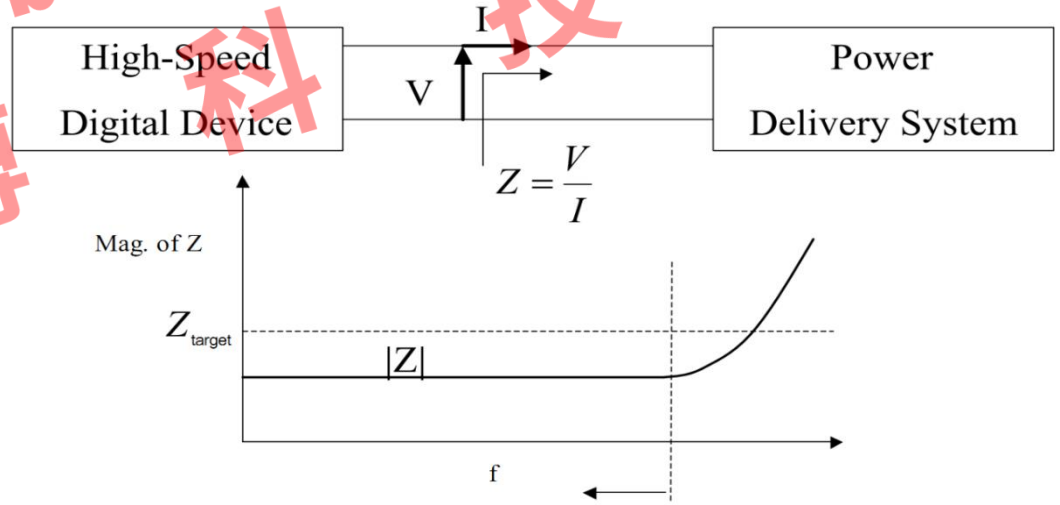
- 时域分析法：直观易懂，但对设计帮助不大





- 频域分析法：略显抽象，却能快速解决问题





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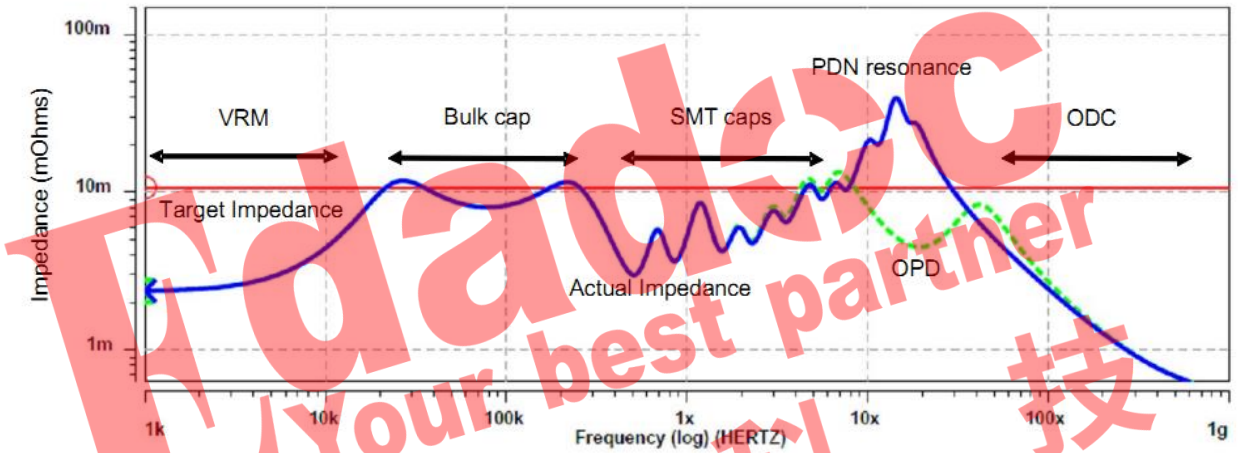
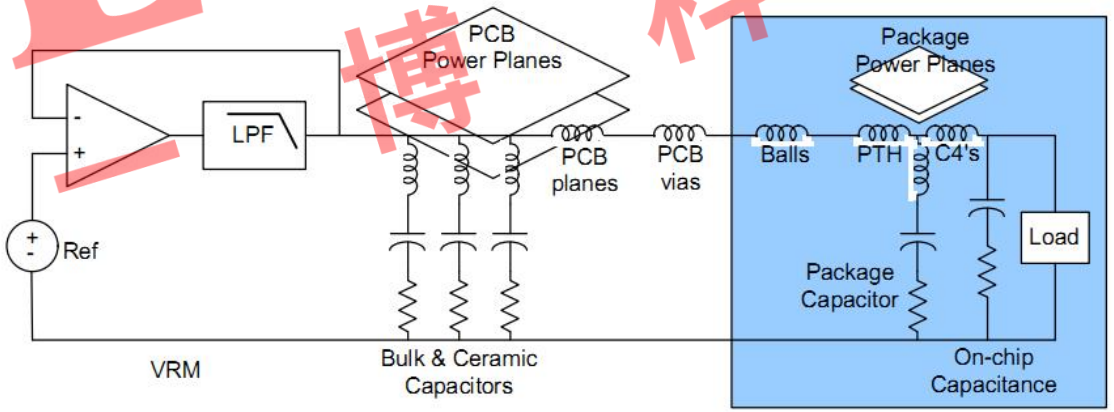
频域分析之目标阻抗法

- 频域分析之目标阻抗法

$$Z_{target} = \frac{(\text{Power Supply Voltage}) \times (\text{allowed ripple})}{\text{current}} = \frac{(5V) \times (5\%)}{1 \text{ amp}} = 0.250 \text{ Ohms}$$





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PART 02

板级的PDN优化

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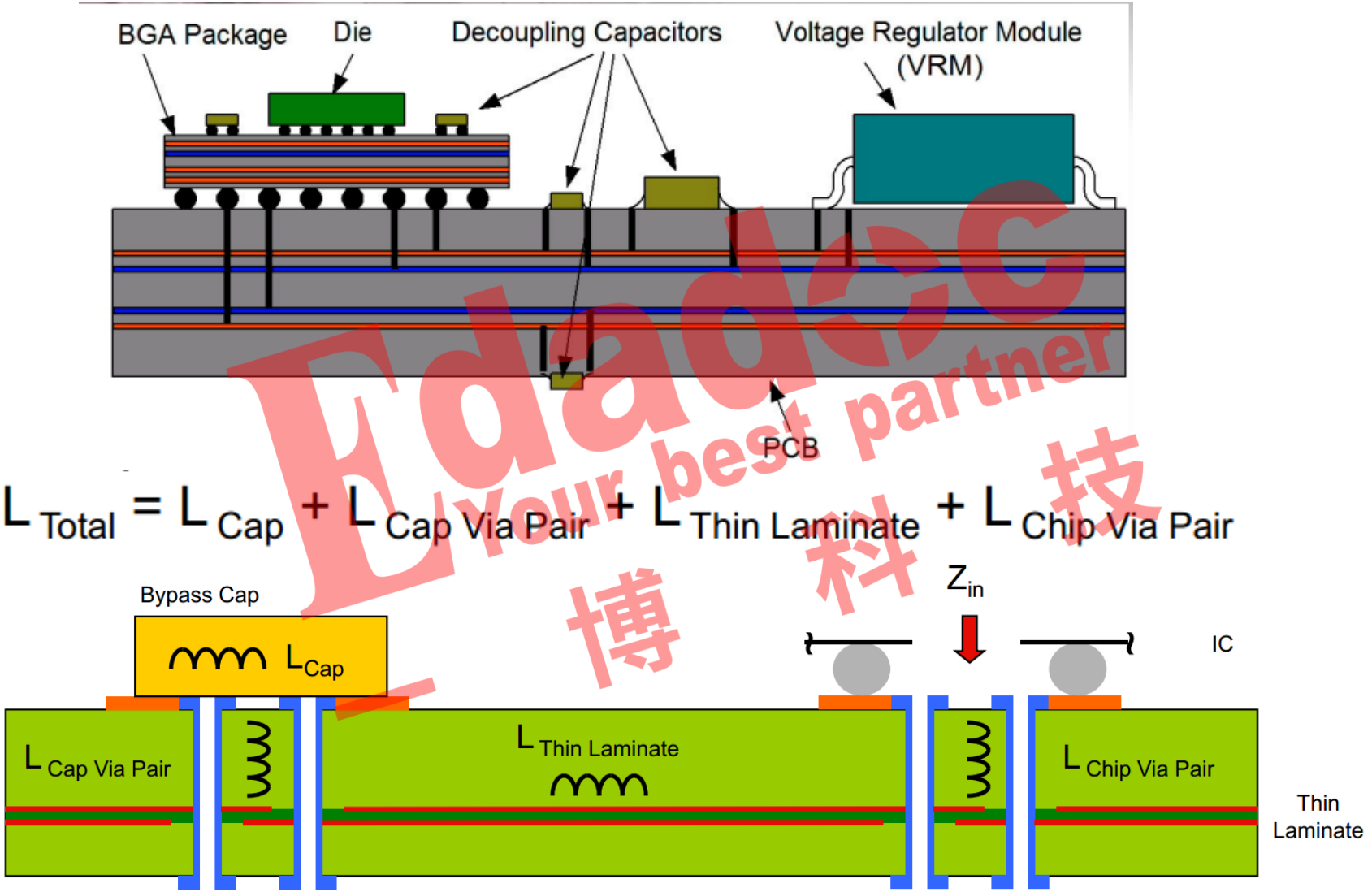
板级的PDN优化

- 板级的PDN优化



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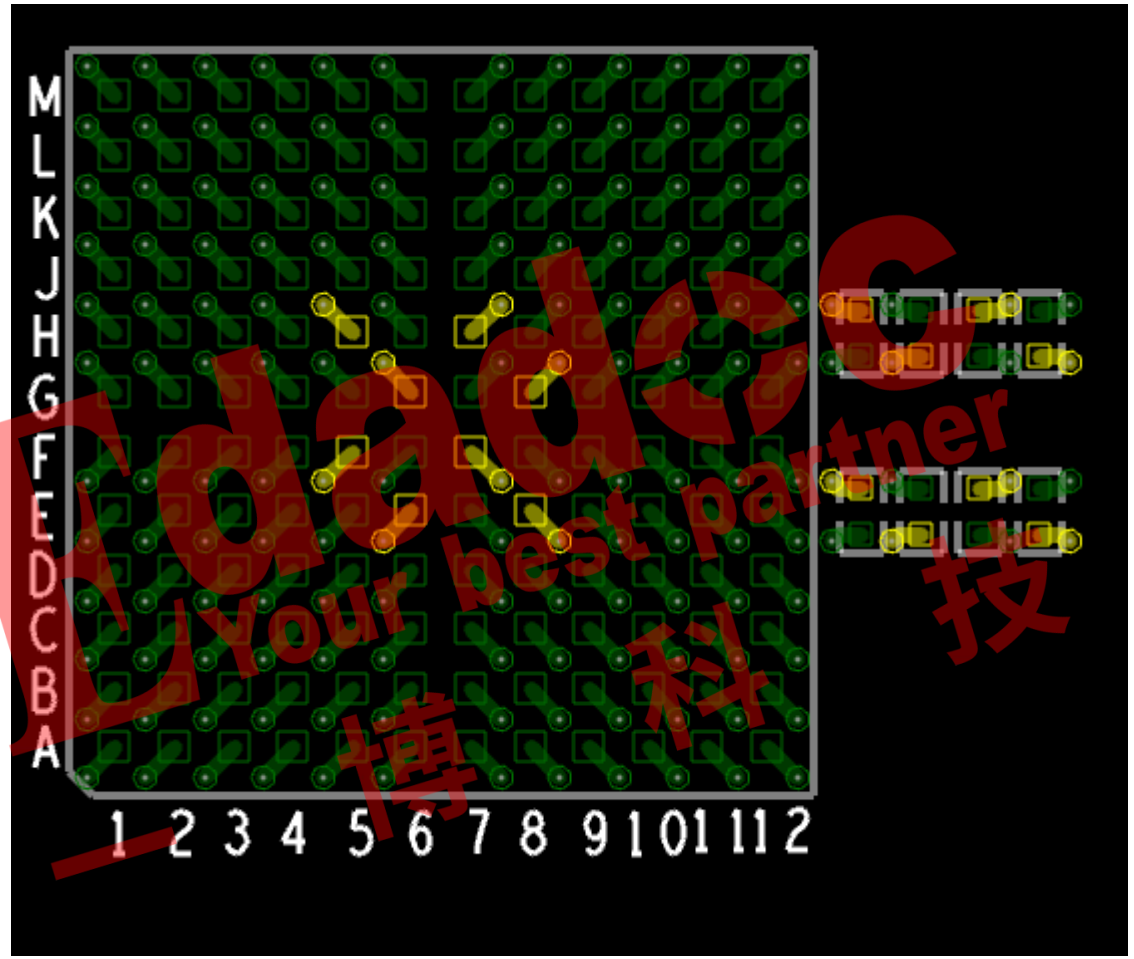
验证板的电容及叠层信息

- 电容容值：0.1μF
- 电容数量：8个
- 电容封装：0402
- 板材使用FR4，板厚3mm，叠层设置如下:

Subclass Name	Type	Material	Thickness (MIL)
	SURFACE	AIR	
TOP	CONDUCTOR	COPPER	1.8
	DIELECTRIC	FR-4	3
GND01	PLANE	COPPER	1.2
	DIELECTRIC	FR-4	3
VCC01	PLANE	COPPER	1.2
	DIELECTRIC	FR-4	5
ART04	CONDUCTOR	COPPER	1.2
	DIELECTRIC	FR-4	32.7
ART05	CONDUCTOR	COPPER	1.2
	DIELECTRIC	FR-4	5
GND06	PLANE	COPPER	1.2
	DIELECTRIC	FR-4	3
GND07	PLANE	COPPER	1.2
	DIELECTRIC	FR-4	5
ART08	CONDUCTOR	COPPER	1.2
	DIELECTRIC	FR-4	32.7
ART09	CONDUCTOR	COPPER	1.2
	DIELECTRIC	FR-4	5
GND10	PLANE	COPPER	1.2
	DIELECTRIC	FR-4	3
GND11	PLANE	COPPER	1.2
	DIELECTRIC	FR-4	3
BOTTOM	CONDUCTOR	COPPER	1.8
	SURFACE	AIR	

一个典型的设计



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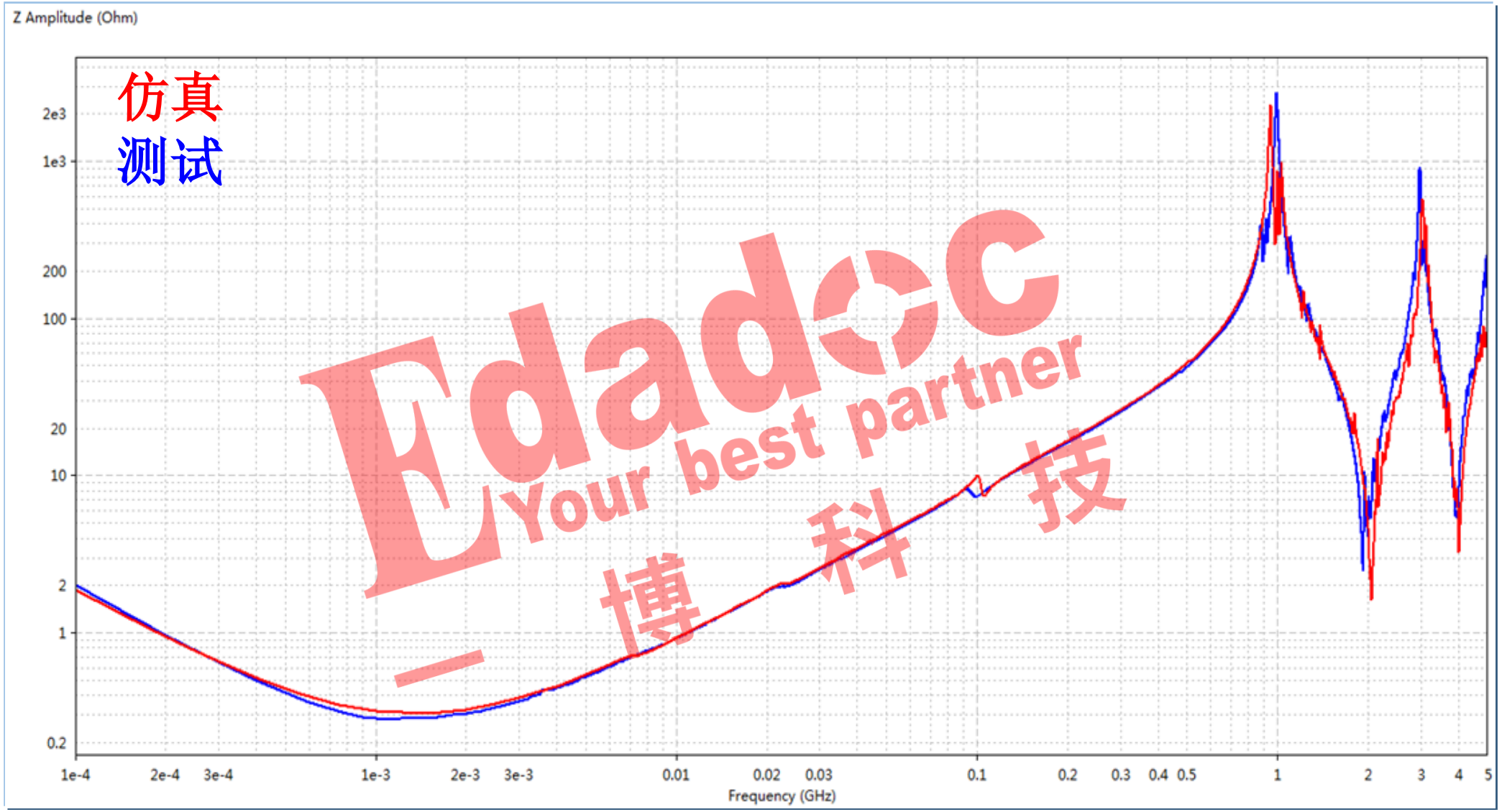
PDN的仿真测试拟合



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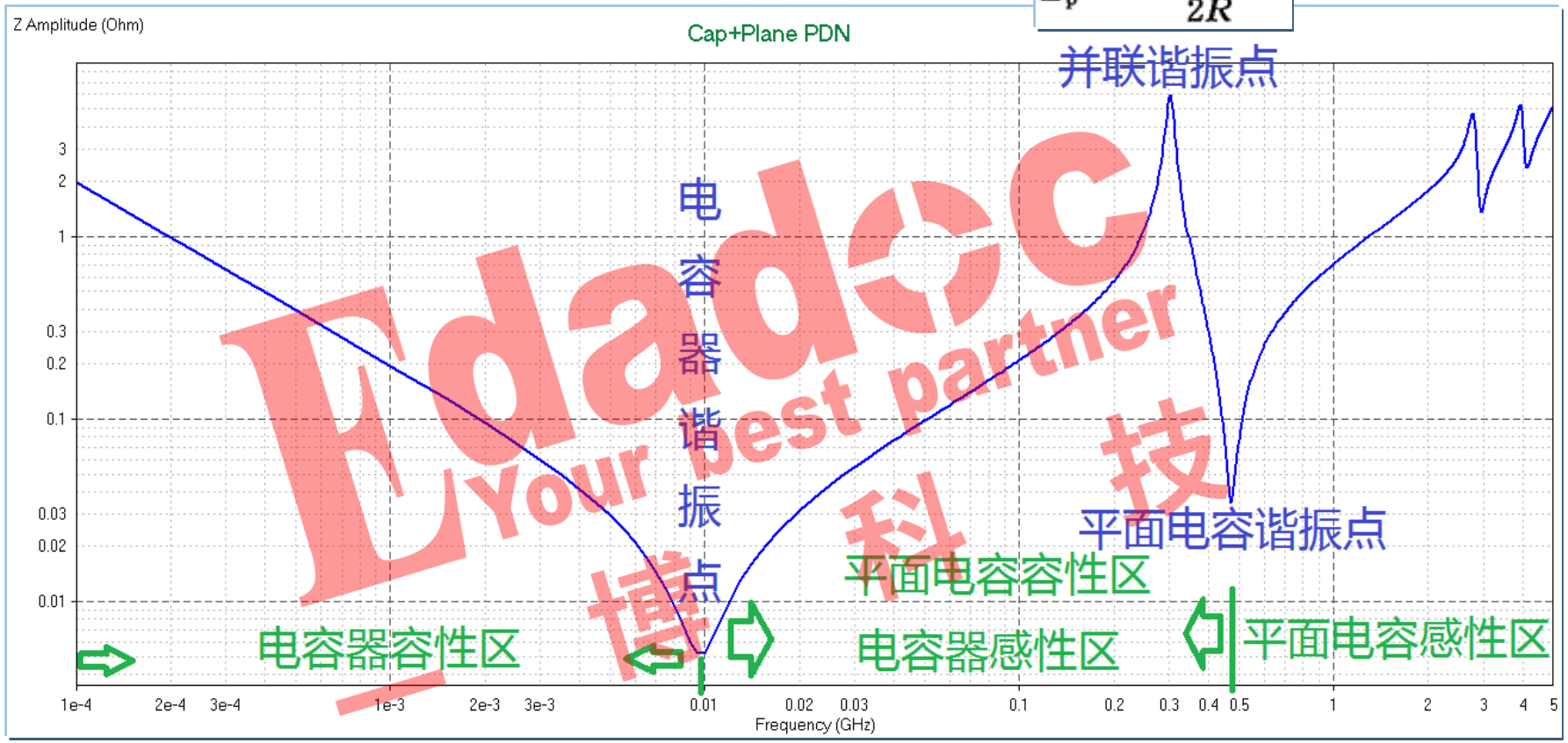
板级去耦系统

$$Z_p = \frac{R^2 + \frac{L}{C}}{2R}$$



$$f_R = \frac{1}{2\pi\sqrt{LC}}$$

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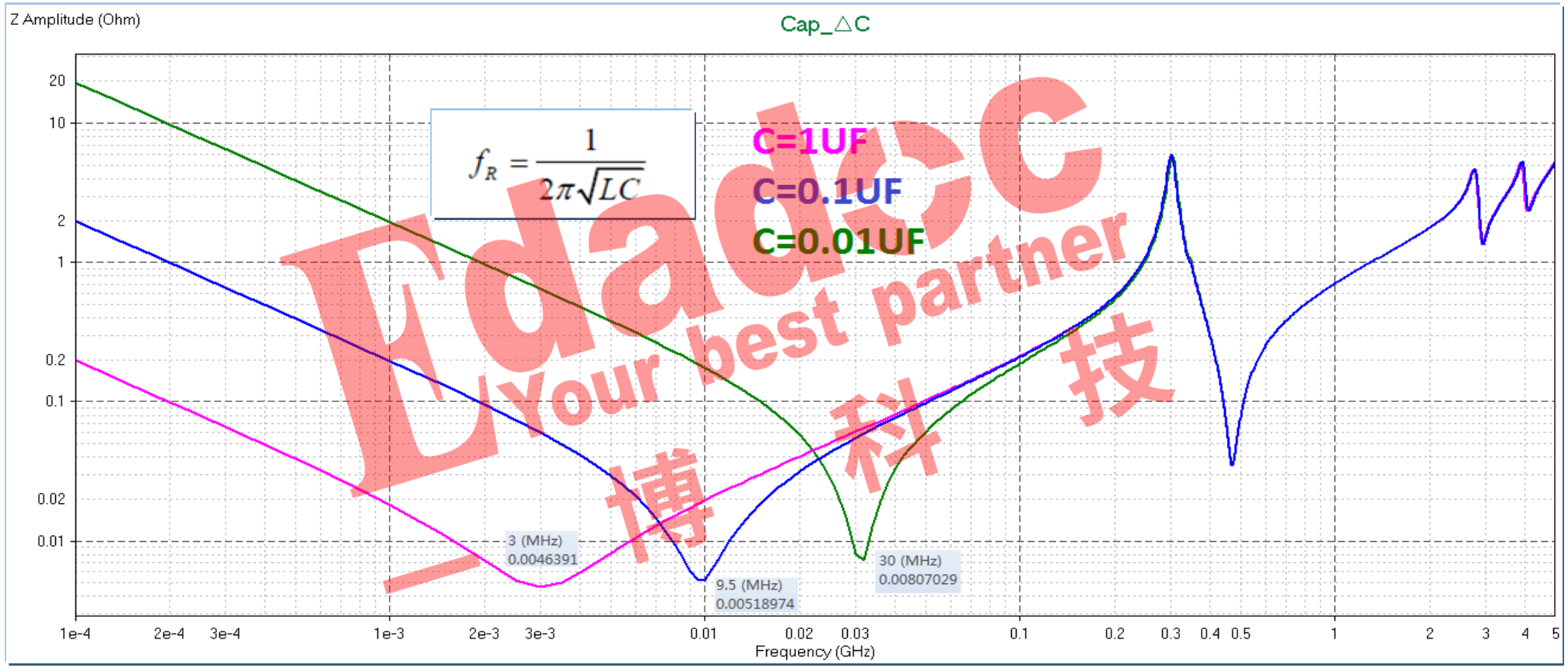
电容容值的影响

- 电容寄生电感（ESL）、寄生电阻（ESR）不变，改变容值



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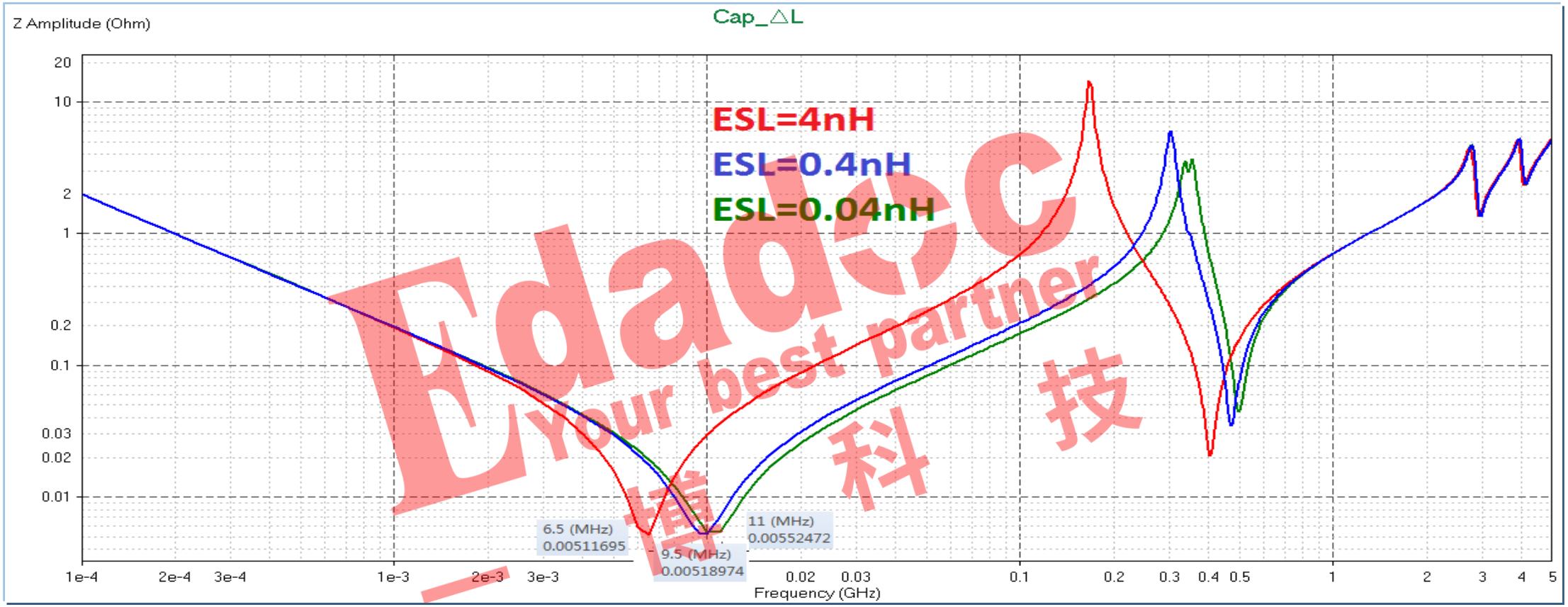
电容寄生电感（ESL）的影响

- 电容容值及ESR保持不变，改变ESL



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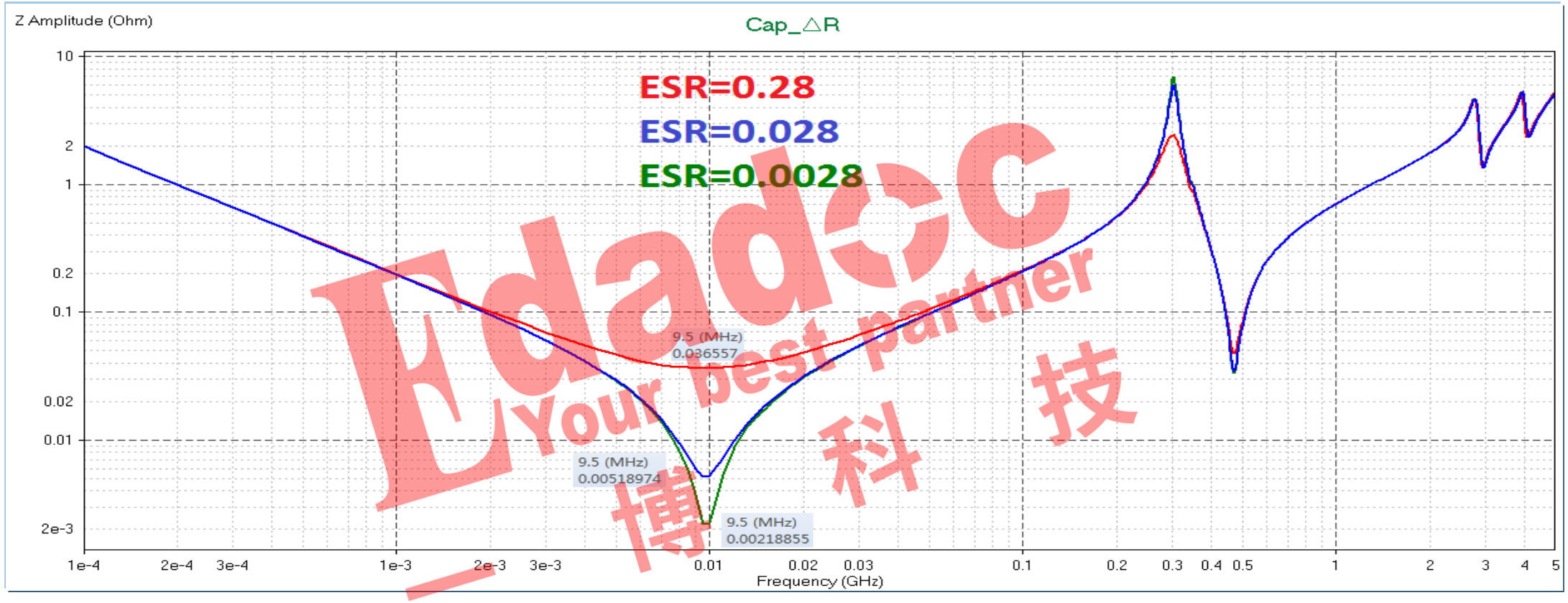
电容寄生电阻（ESR）的影响

- 电容容值及ESL保持不变，改变ESR



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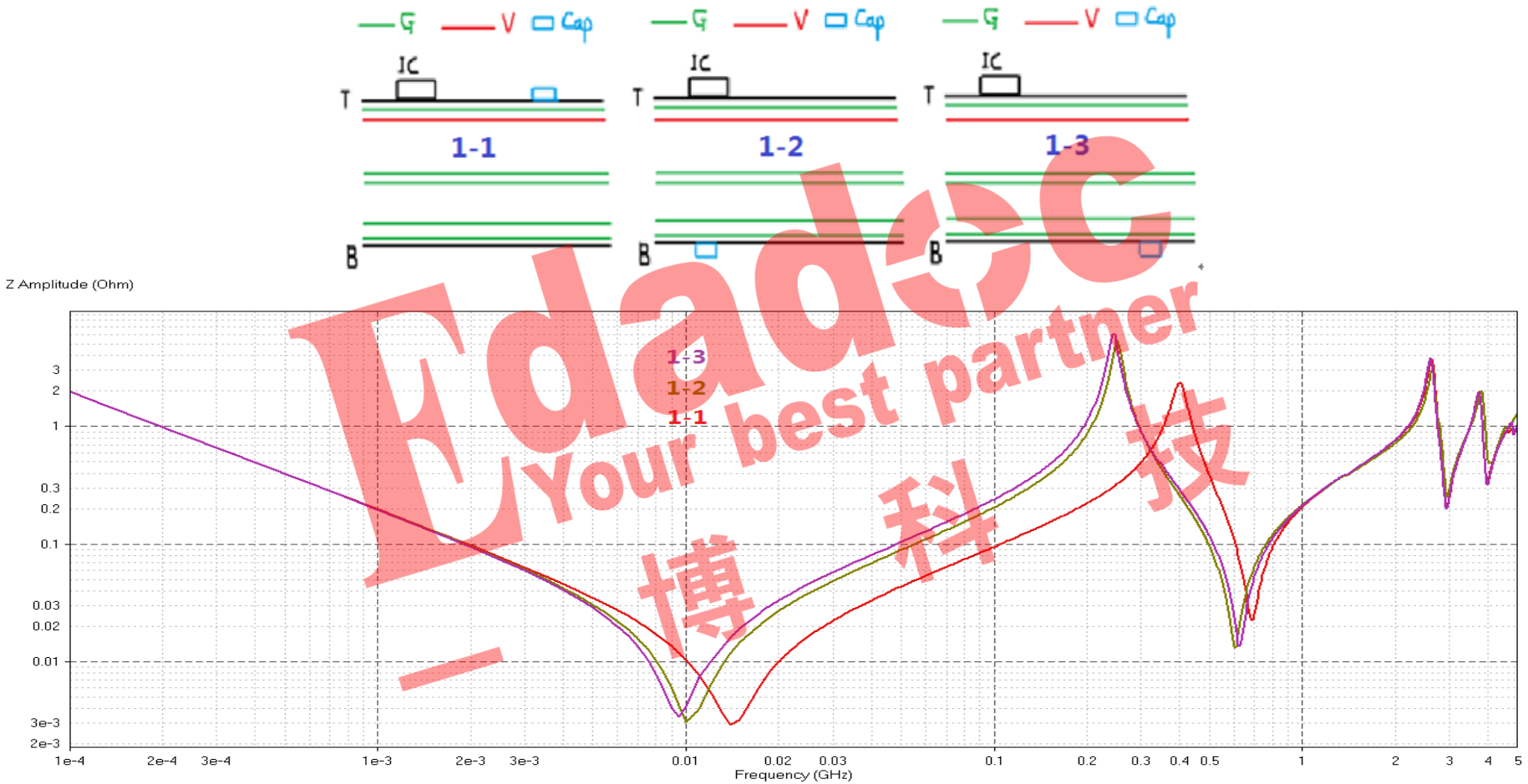
一些有意思的设计对比

- 电源平面靠近IC布局面时的三种电容位置的PDN阻抗



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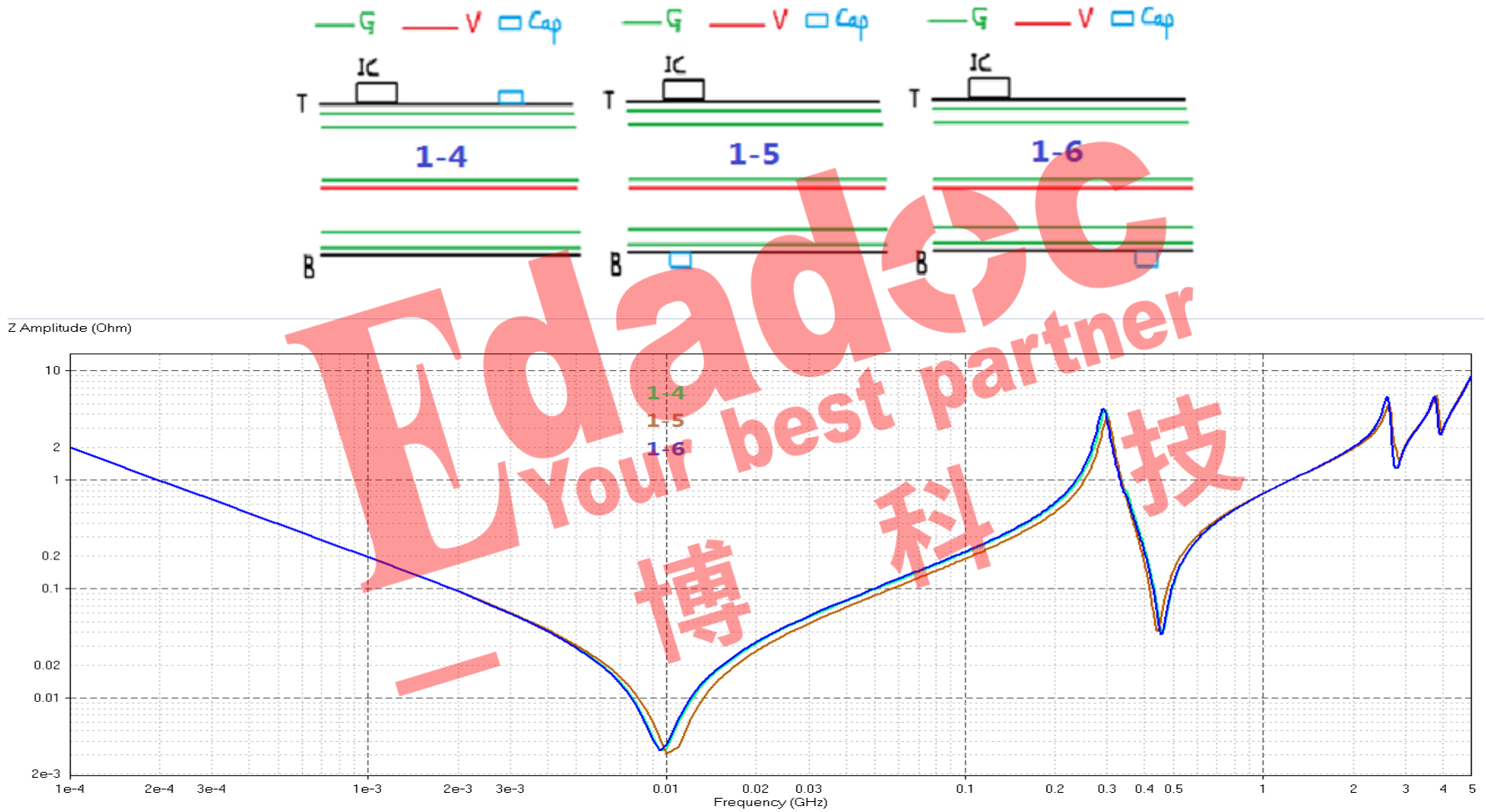
一些有意思的设计对比

- 电源平面位于叠层中间时三种电容位置的PDN



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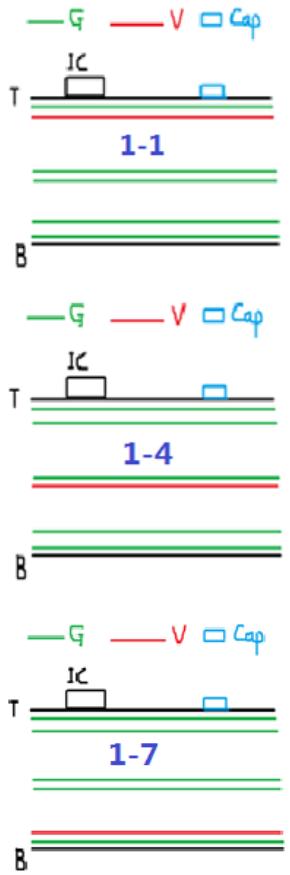
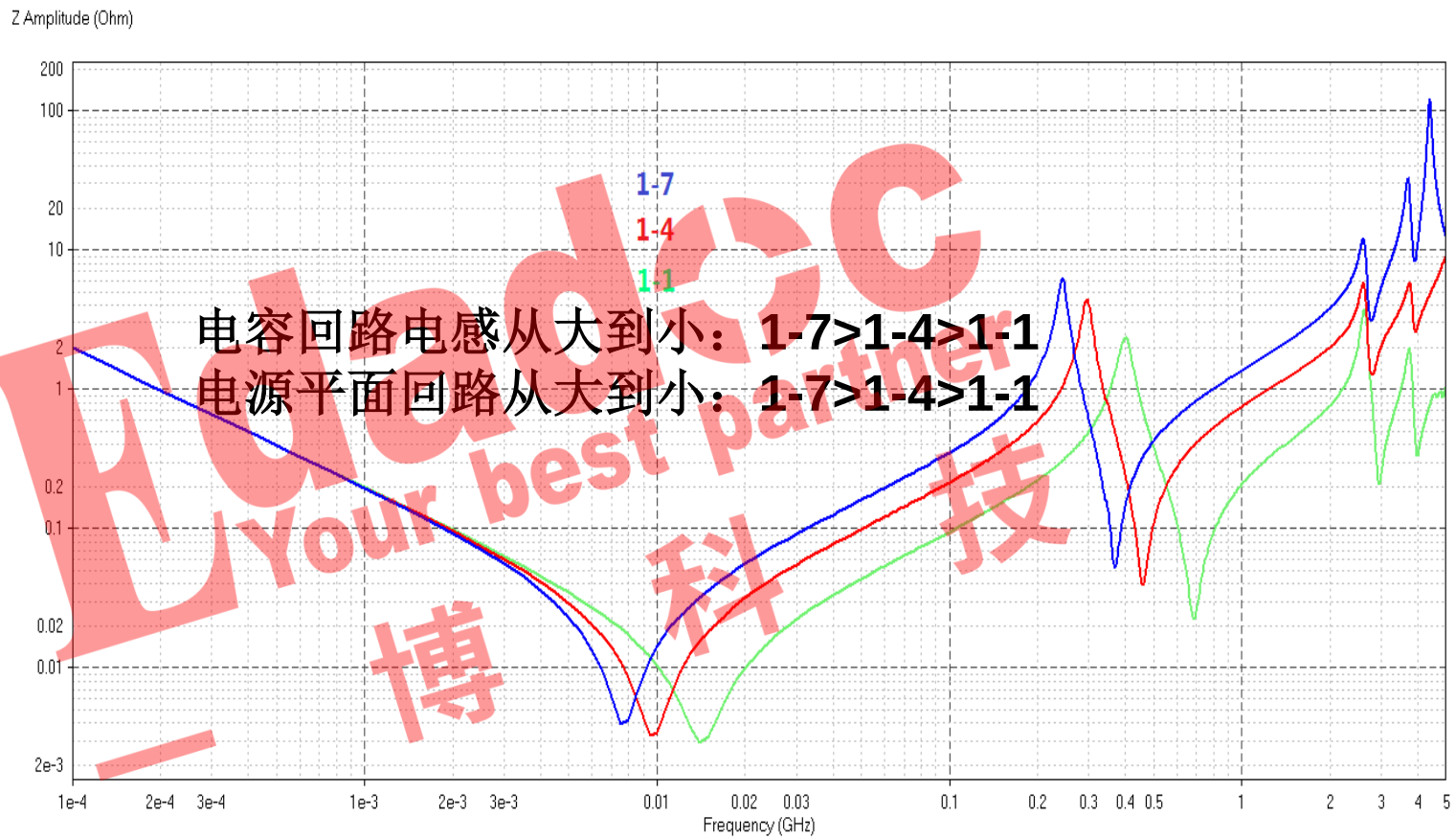
一些有意思的设计对比

- 确定电容位置，改变电源平面在叠层中位置





电容回路电感从大到小：1-7>1-4>1-1

电源平面回路从大到小：1-7>1-4>1-1

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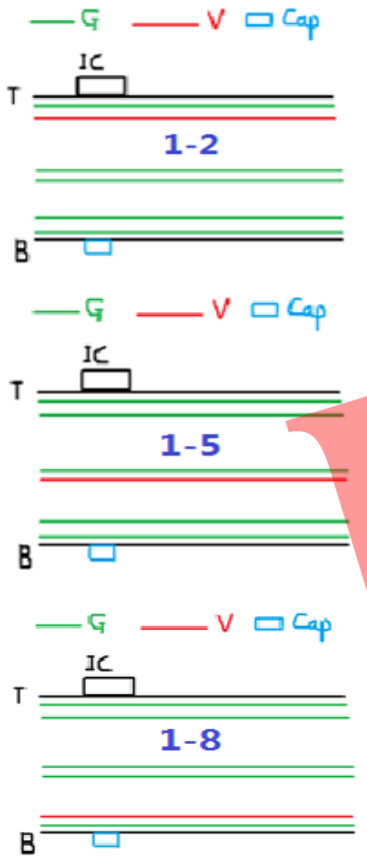
一些有意思的设计对比

- 确定电容位置，改变电源平面在叠层中位置



电容回路电感基本相等
电源平面回路电感从大到小：1-8>1-5>1-2
电源平面电容从大到小：1-5>1-8 ≈1-2

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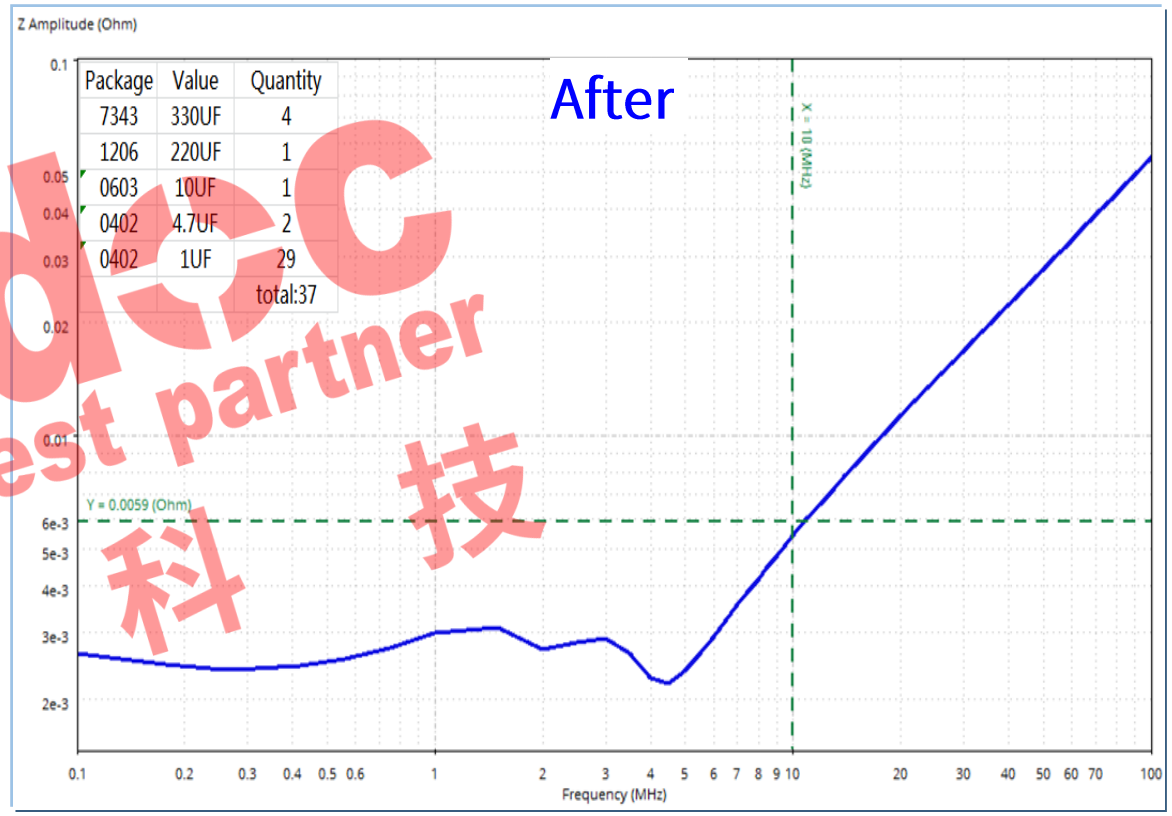
调整容值案例

- 电容配置的总数量不变，容值组合调整



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电源PDN设计总结

- 电容组合选择最重要，决定了PDN的性能
- 电源平面层叠设计不容忽视
- 电容自身Fan out设计，细节需要注意
- 成熟的芯片设计指导书，会给出电容设计的详细要求

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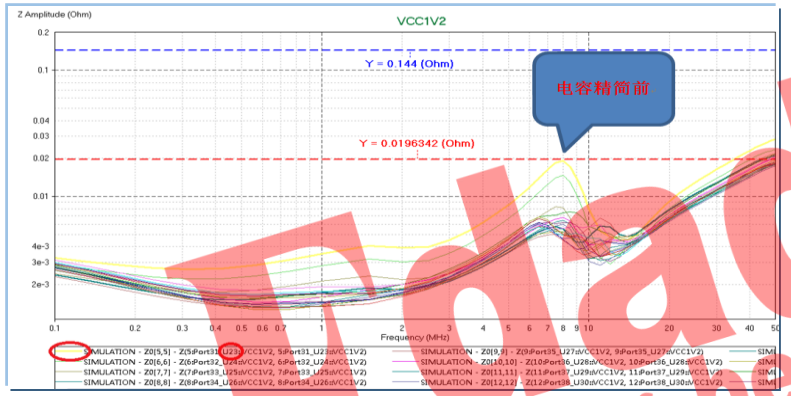
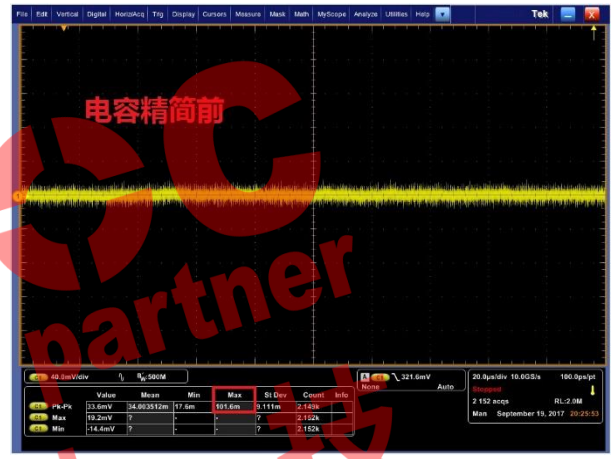
电容精简案例

- 电容配置的容值组合不变，电容数量精简：

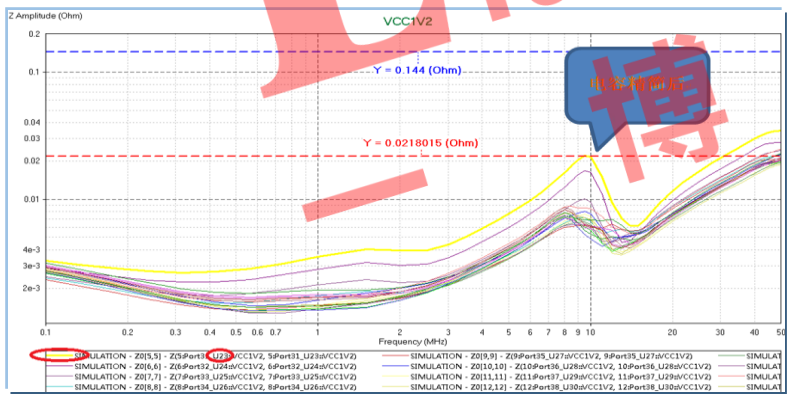
  20颗DDR芯片，每个DDR颗粒精简5个0.1μF电容，共精简100个电容

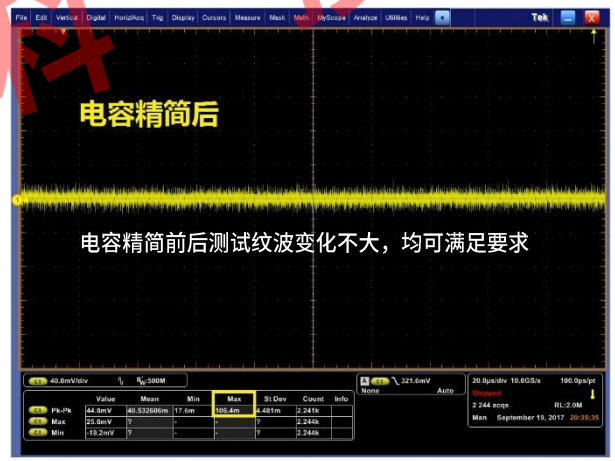
Before





After





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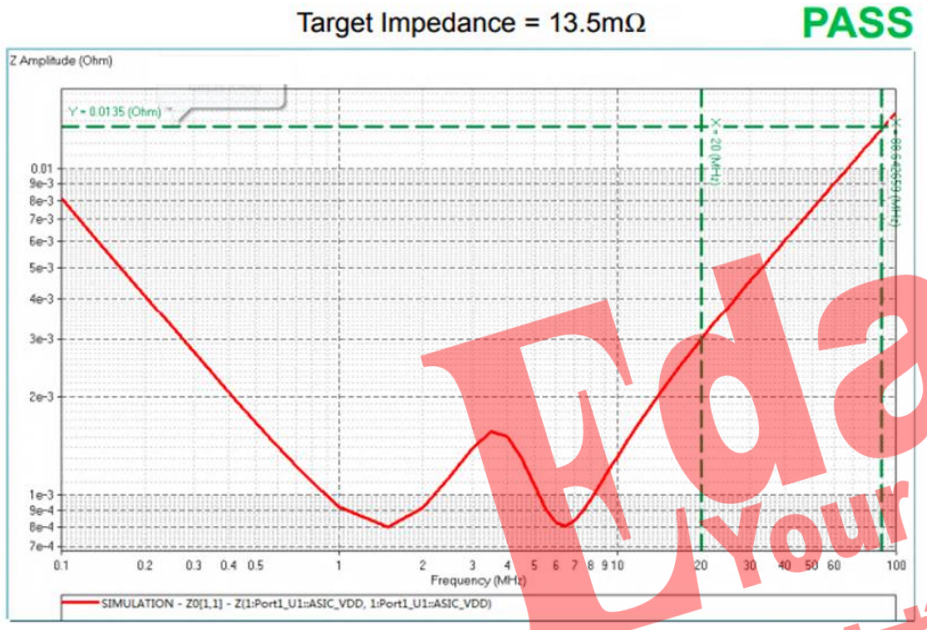
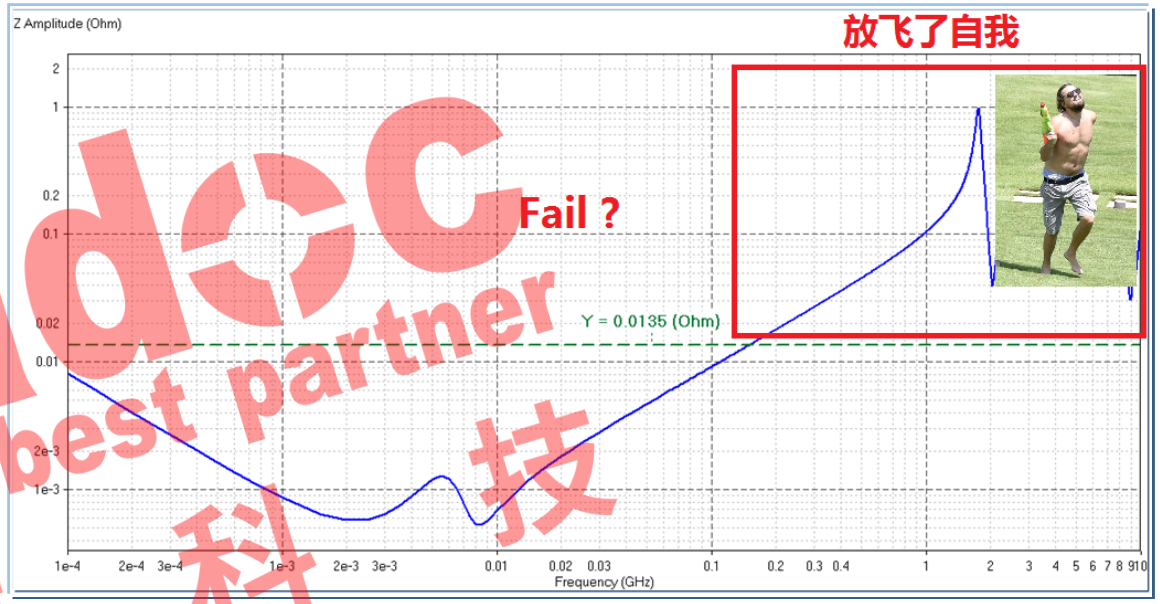
Part 03

全链路PDN阻抗优化案例

板级PDN仿真为何只看到100MHz

- 因为你看到100MHz后的PDN阻抗会崩溃





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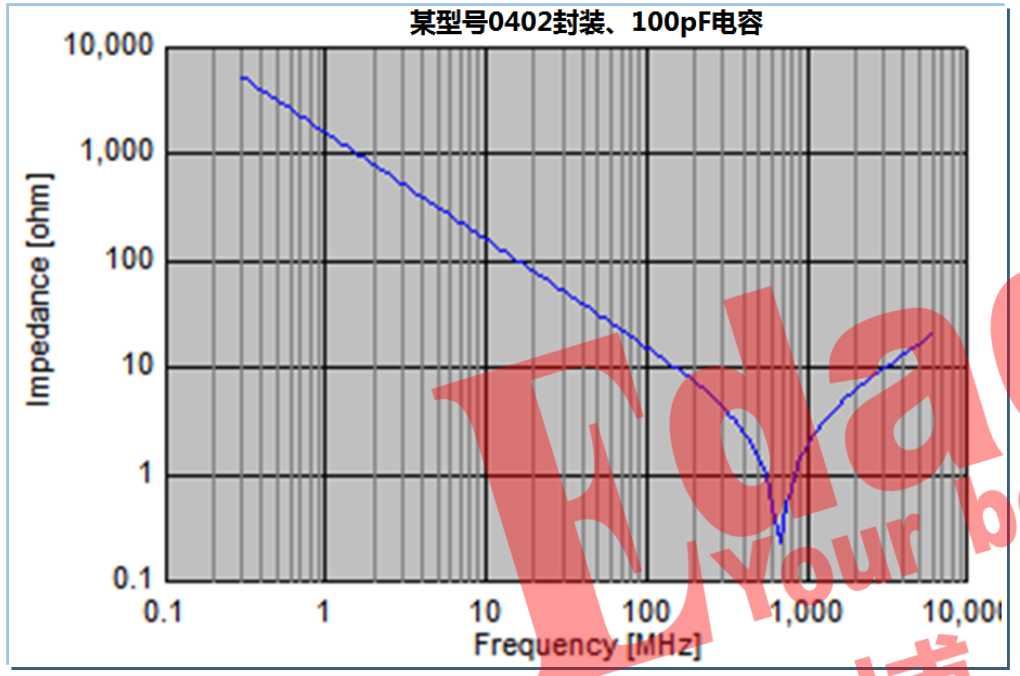
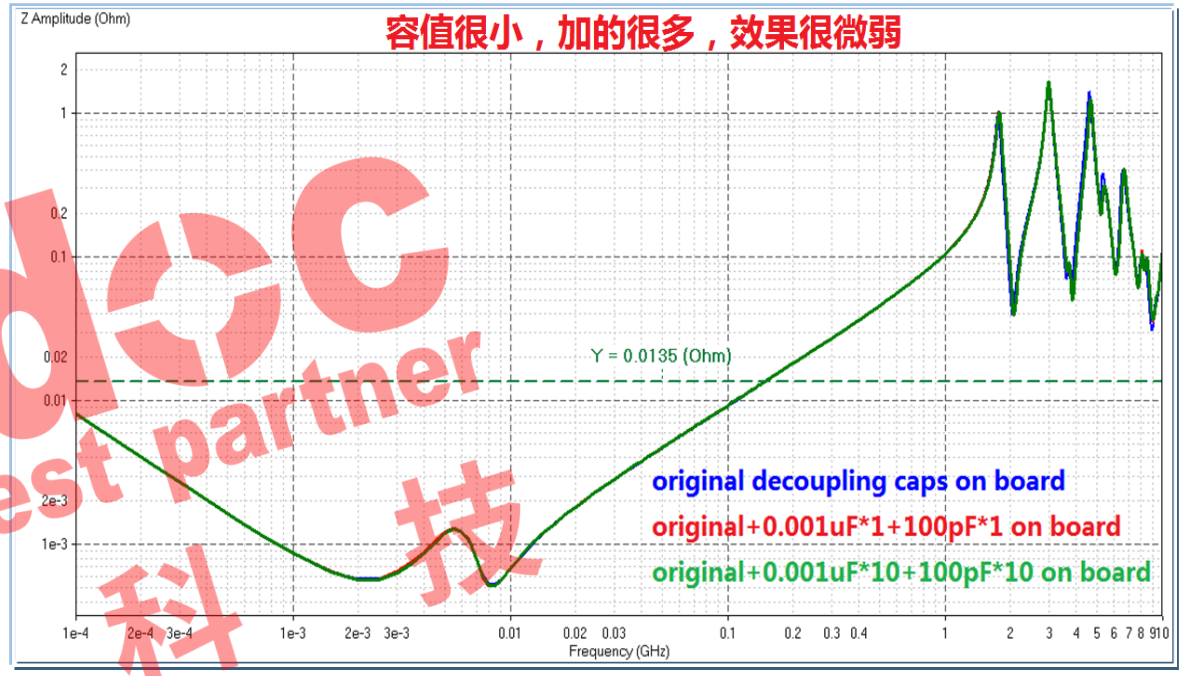
板级小容值电容的去耦效果

- 板级小容值电容能解决高频段的去耦吗?





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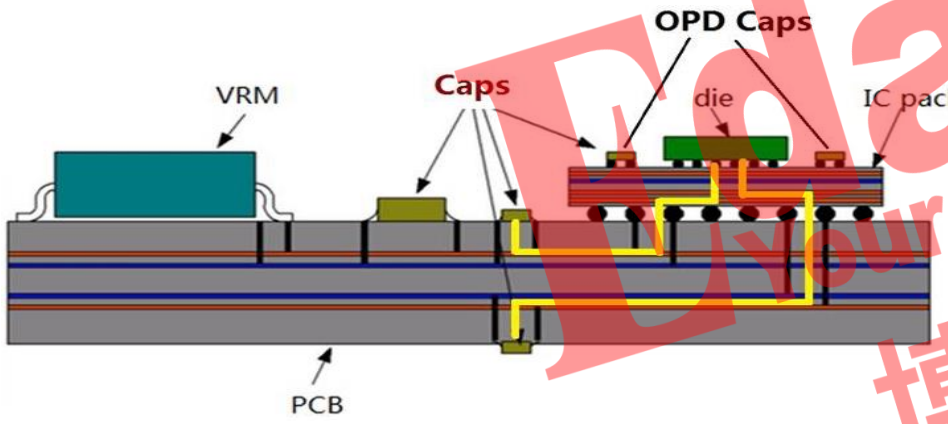
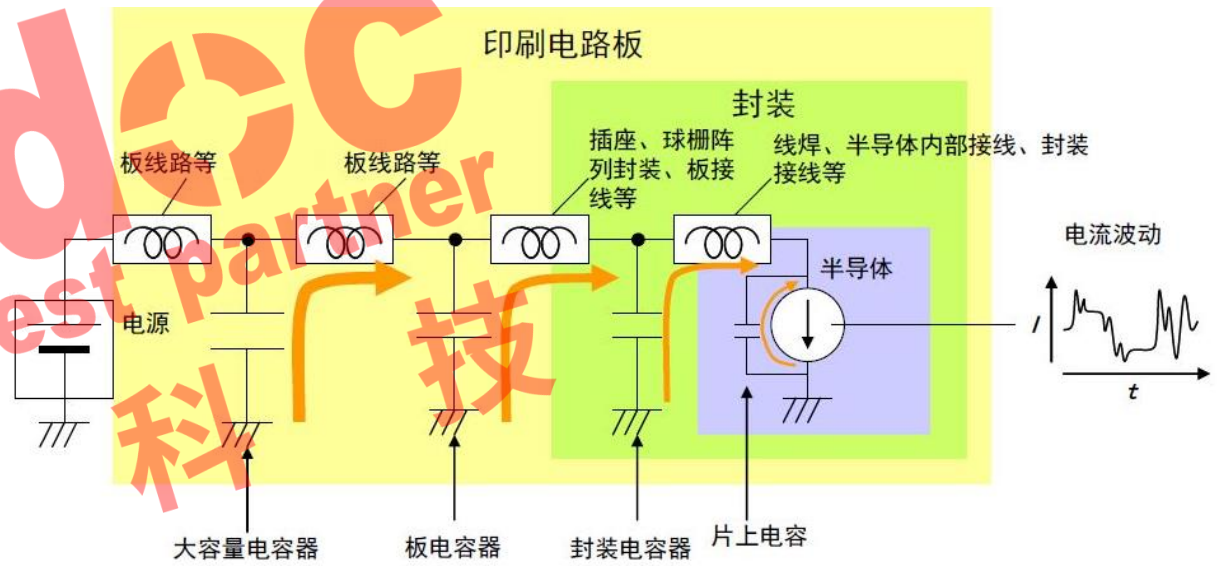
电感！还是电感！

- 不仅有寄生电感ESL，还有安装电感Lmount

$$f_{mount} = \frac{1}{2\pi\sqrt{L_{total} \cdot C}} = \frac{1}{2\pi\sqrt{(ESL + L_{mount}) \cdot C}}$$





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频段分工，高频段去耦到底归谁管？

- 内心是崩溃的

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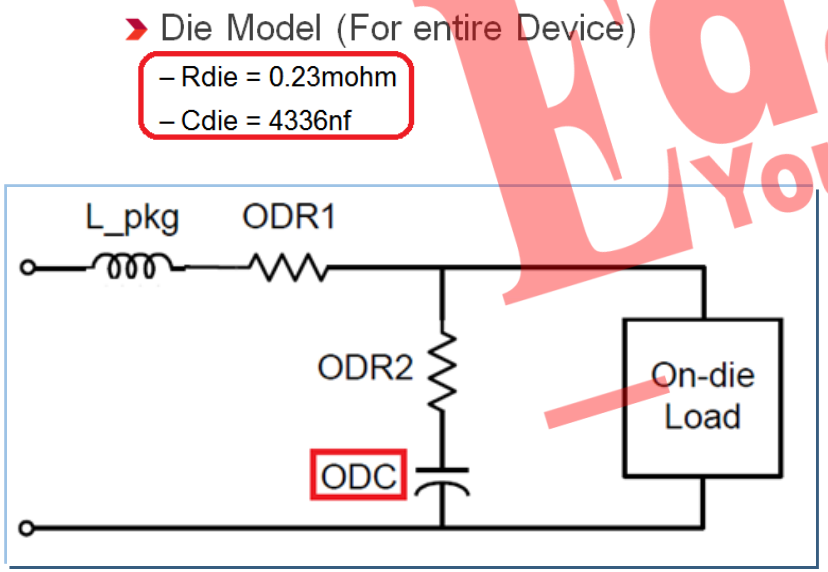
片上电容简介

- 电源和地轨道金属层之间的电容
- 扩散电容
- 栅极电容
- 其它

显著优点：寄生电感（ESL）基本可忽略！



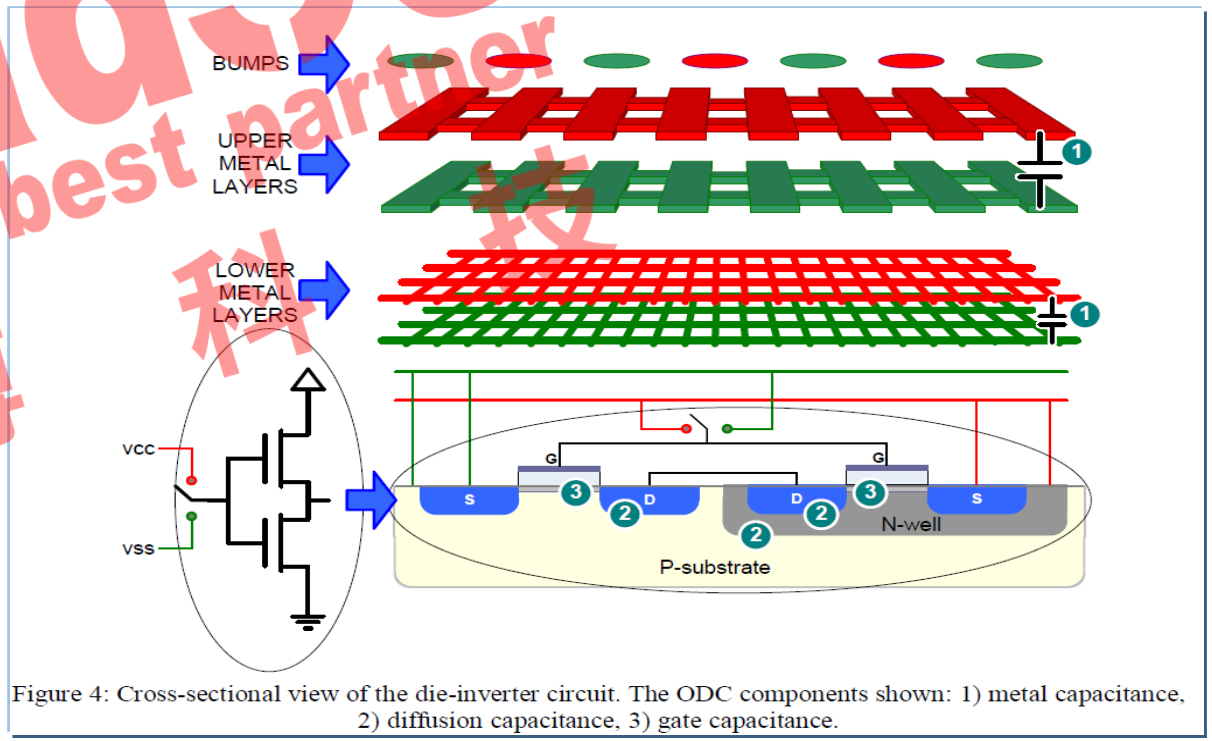


Figure 4: Cross-sectional view of the die-inverter circuit. The ODC components shown: 1) metal capacitance, 2) diffusion capacitance, 3) gate capacitance.

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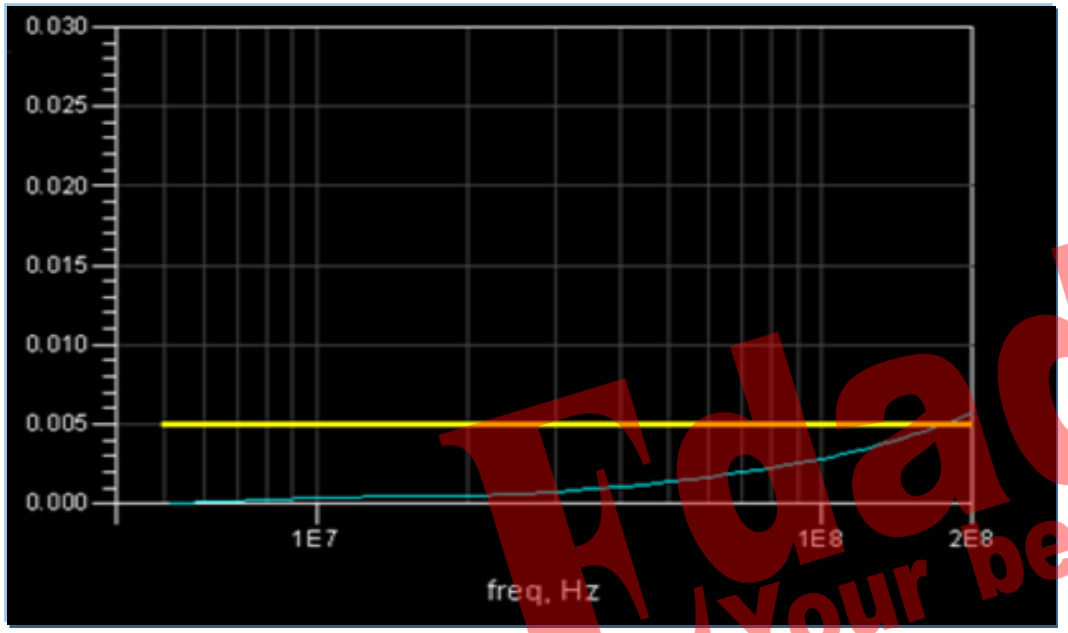
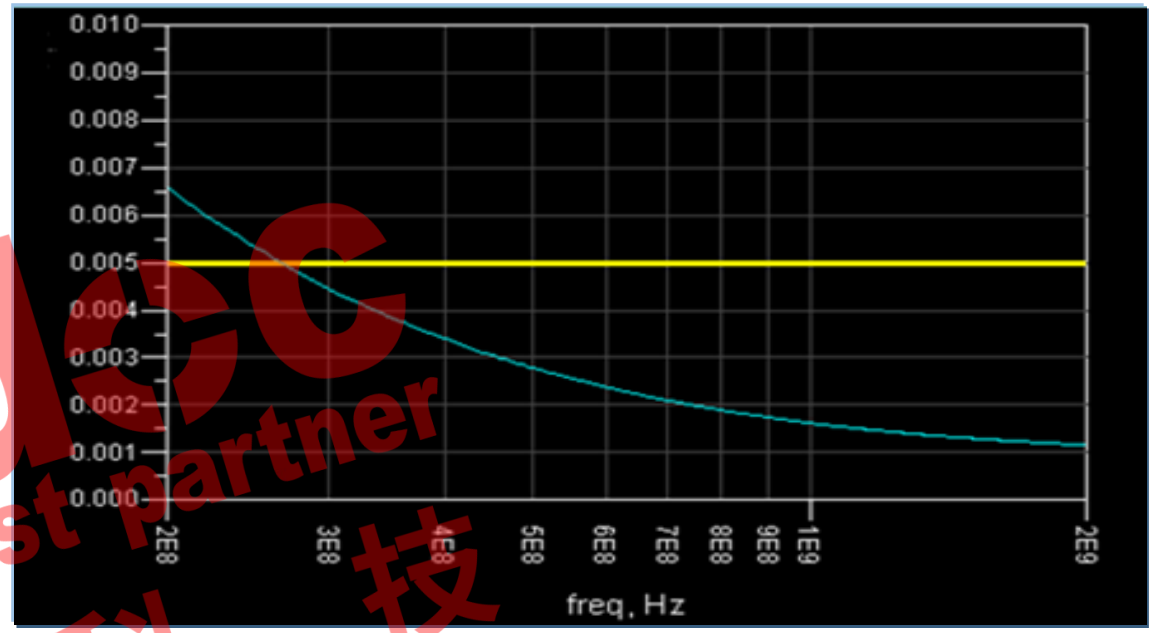
全链路PDN优化案例

该电源目标阻抗Z_{target}=5mohm



PCB板级PDN阻抗，100KHz-200MHz



仅封装去耦+die的PDN阻抗，200MHz-2GHz

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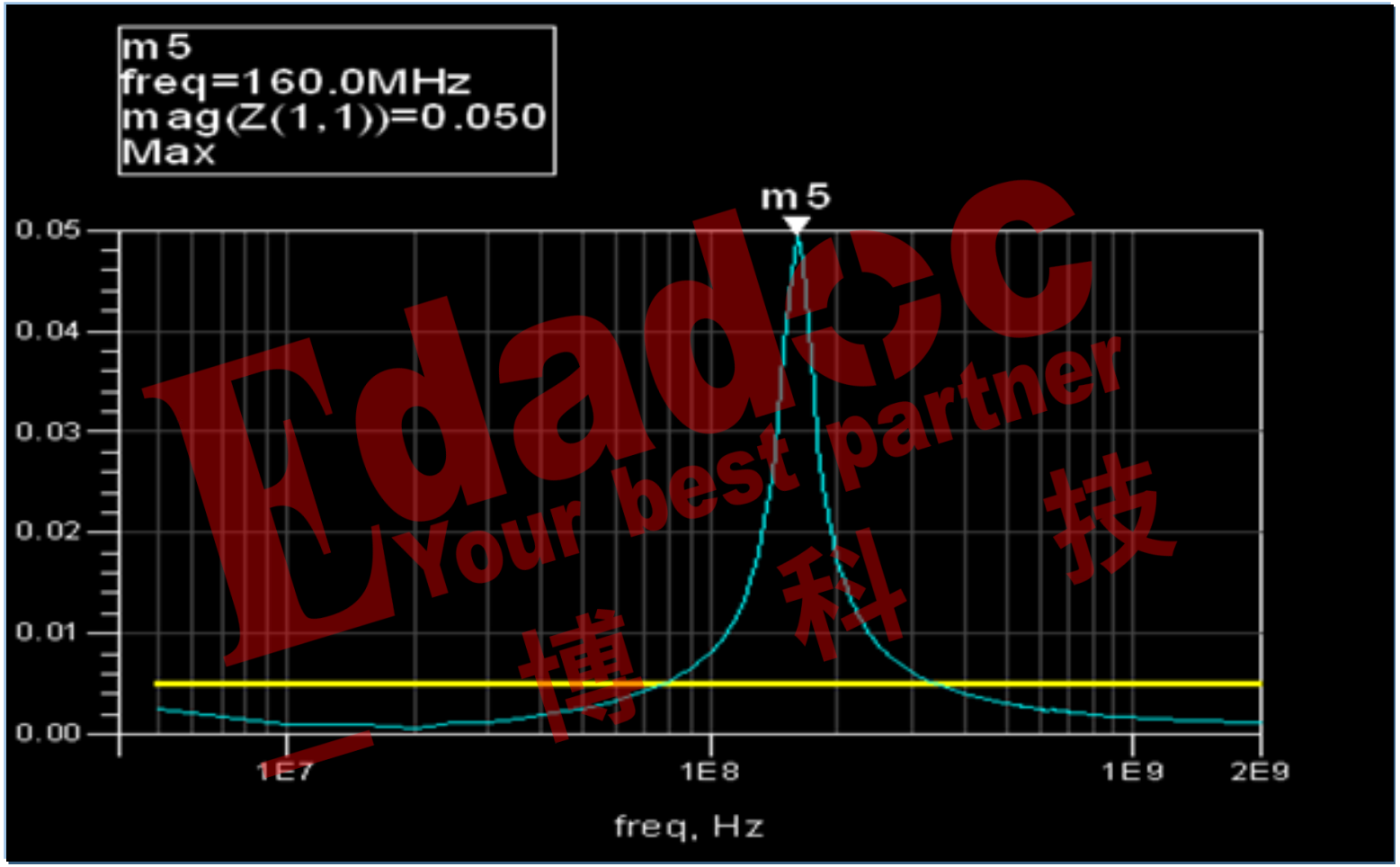
全链路PDN优化案例

PCB板级+封装+die的PDN阻抗



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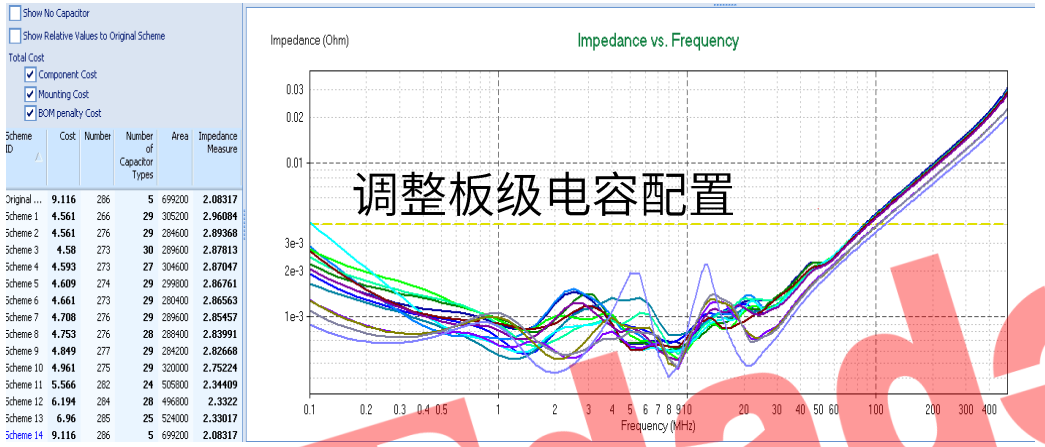
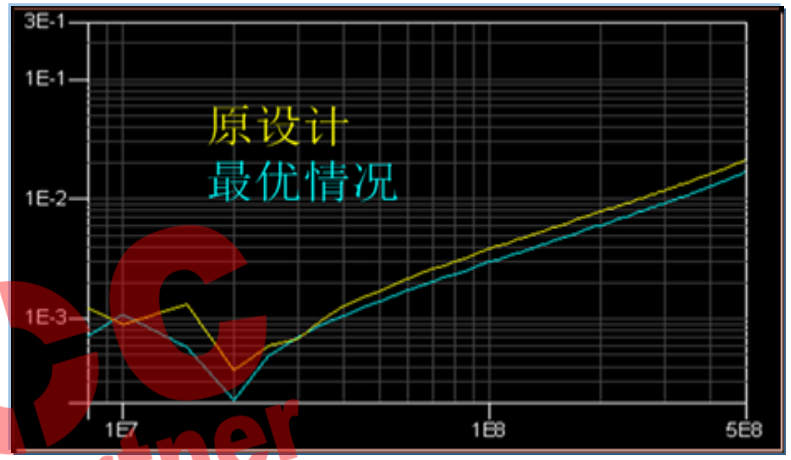
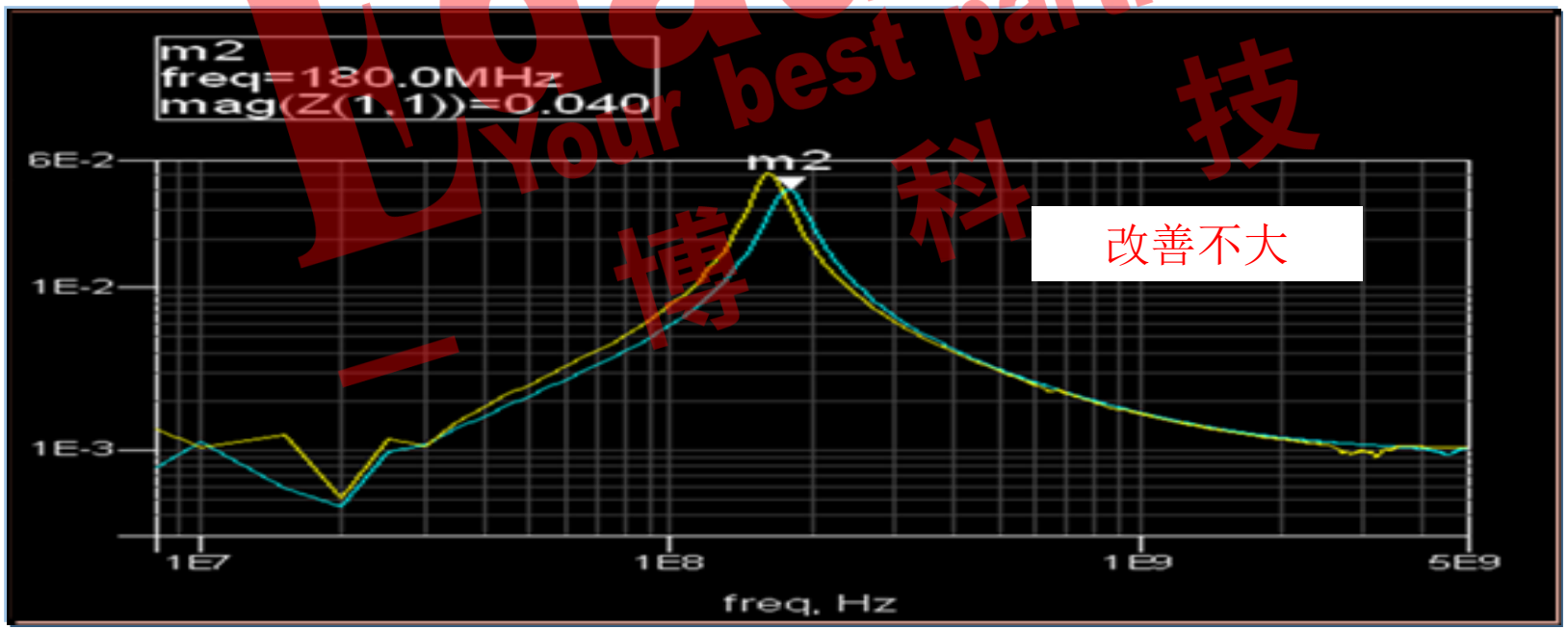
全链路PDN优化案例

- 尝试通过调整板级电容进行改善



Scheme ID	Cost	Number	Number of Capacitor Types	Area	Impedance Measure
Original ...	9.116	286	5	699200	2.08317
Scheme 1	4.561	266	29	305200	2.96084
Scheme 2	4.561	276	29	284600	2.89368
Scheme 3	4.58	273	30	289600	2.87813
Scheme 4	4.593	273	27	304600	2.87047
Scheme 5	4.609	274	29	299800	2.86761
Scheme 6	4.661	273	29	280400	2.86563
Scheme 7	4.708	276	29	289600	2.85457
Scheme 8	4.753	276	28	288400	2.83991
Scheme 9	4.849	277	29	284200	2.82668
Scheme 10	4.961	275	29	320000	2.75224
Scheme 11	5.566	282	24	505800	2.34409
Scheme 12	6.194	284	28	496800	2.3322
Scheme 13	6.96	285	25	524000	2.33017
Scheme 14	9.116	286	5	699200	2.08317





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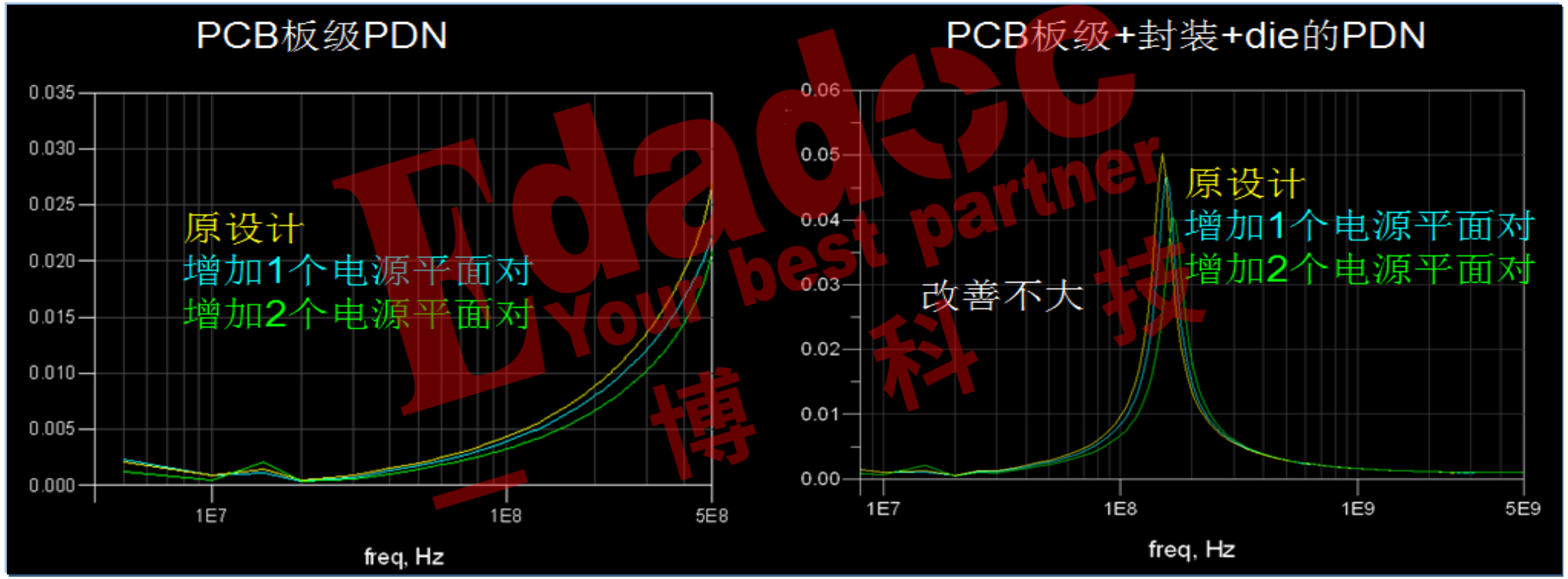
全链路PDN优化案例

- 尝试通过增加平面电容进行改善
- 增加电源平面对



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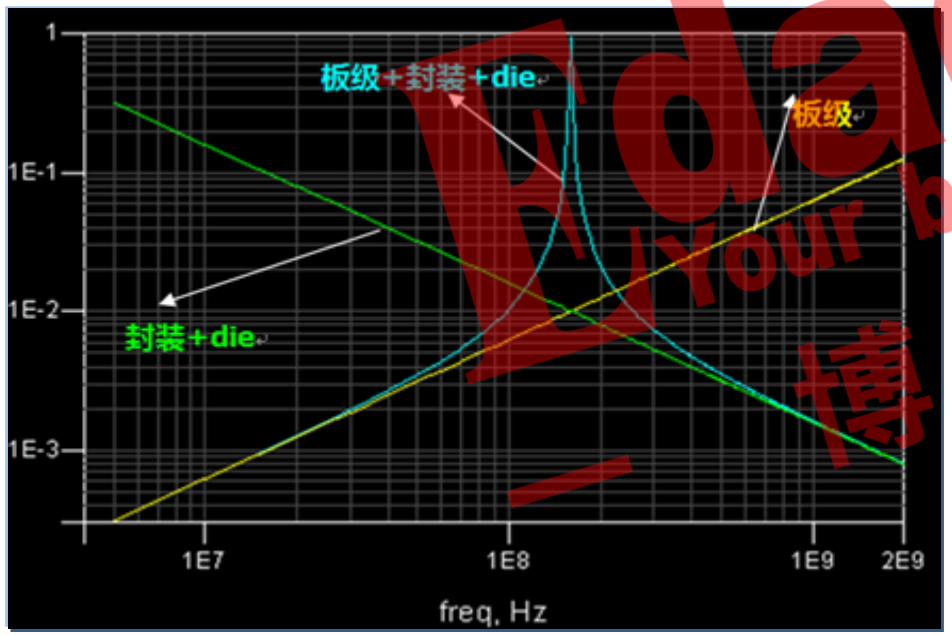
全链路PDN优化案例

- 原理分析



理论解决方法有三个：

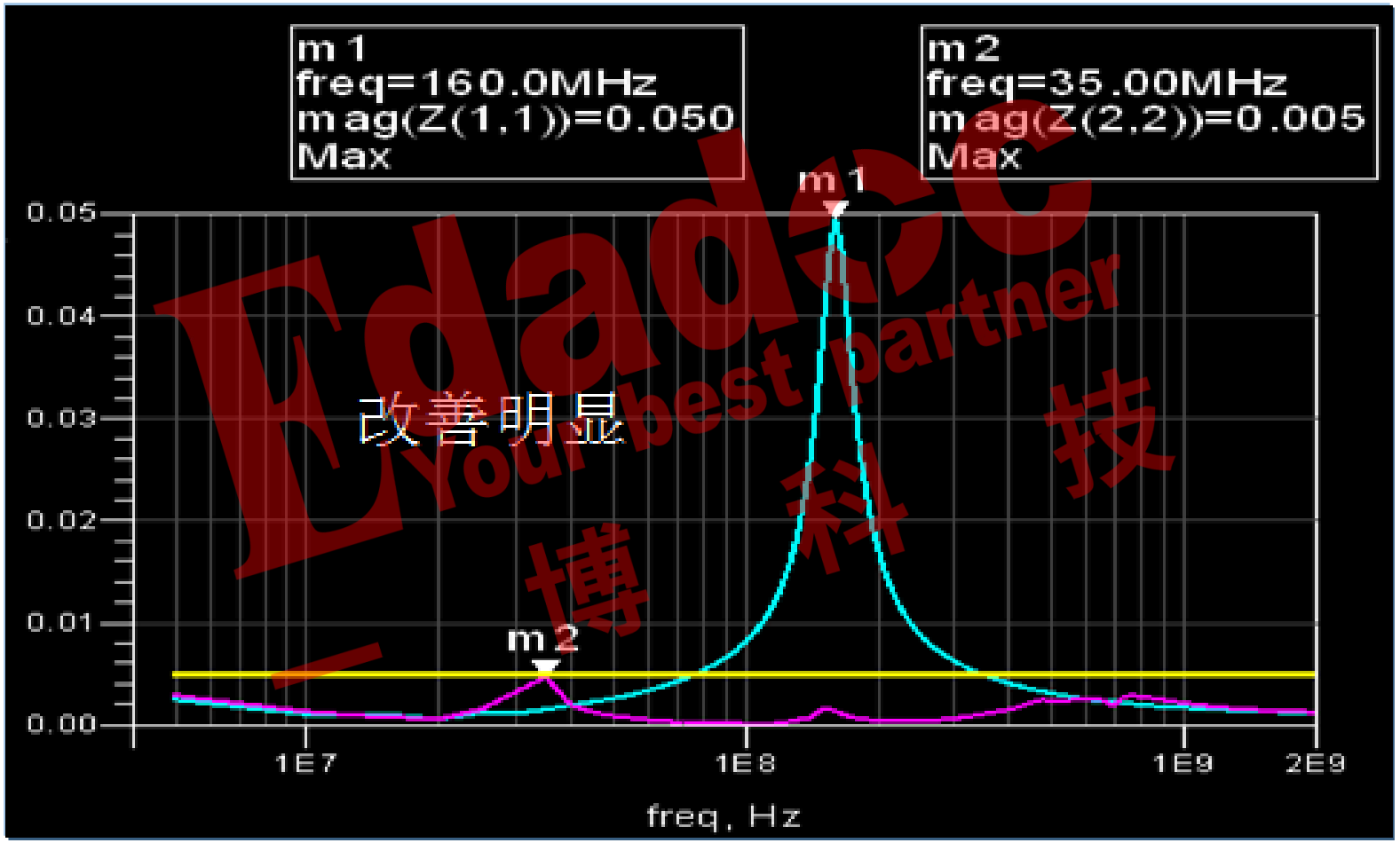
1， 减小L的值---即通过减小板级的电感，增加地平面对改善不大；

2， 增加C的值---即增加die的电容，但是die电容在芯片完成后已经固定，不可能增加；

3， 在L和C中间并联LC的结构，改变原来谐振的位置---即在封装板上加电容。

全链路PDN优化案例

- 增加封装电容（OPD），改善明显



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Part 04

全链路电源纹波优化

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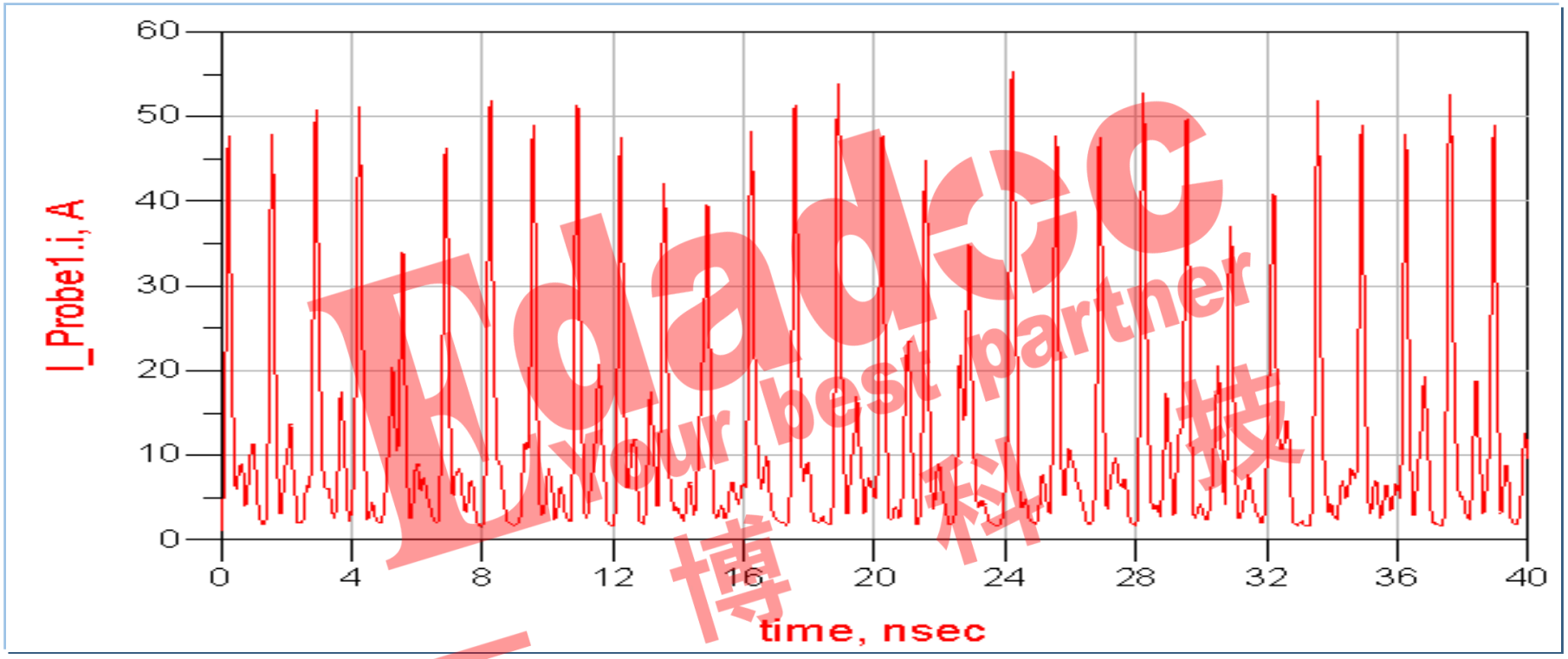
CPM电流及目标阻抗设定

- 根据CPM模型的电流大小，对目标阻抗进行设定：
- Z=0.9V*10%/40A=2.25mohm（按照10%的电压波动，最大变化电流40A计算）



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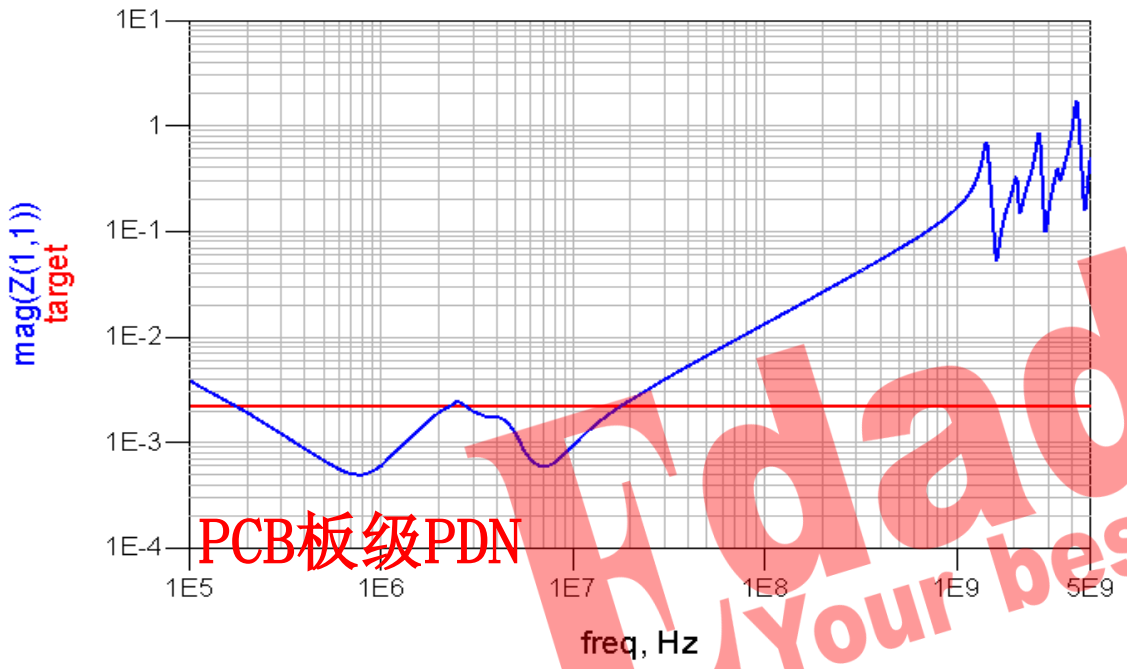
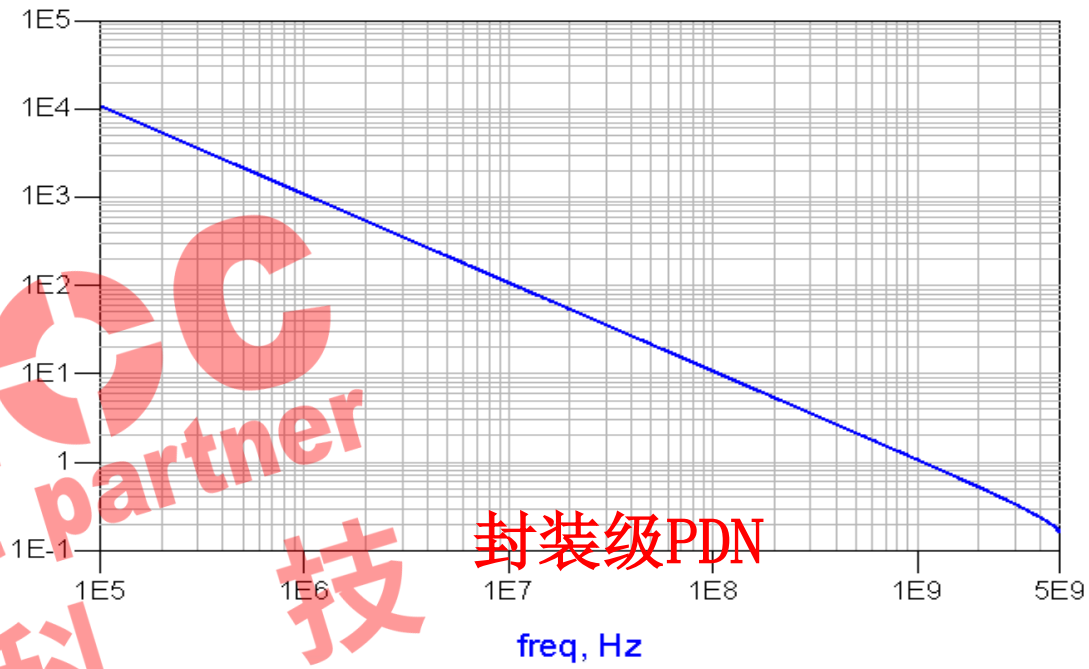
原始设计仿真结果

- 原始PCB和封装设计的结果





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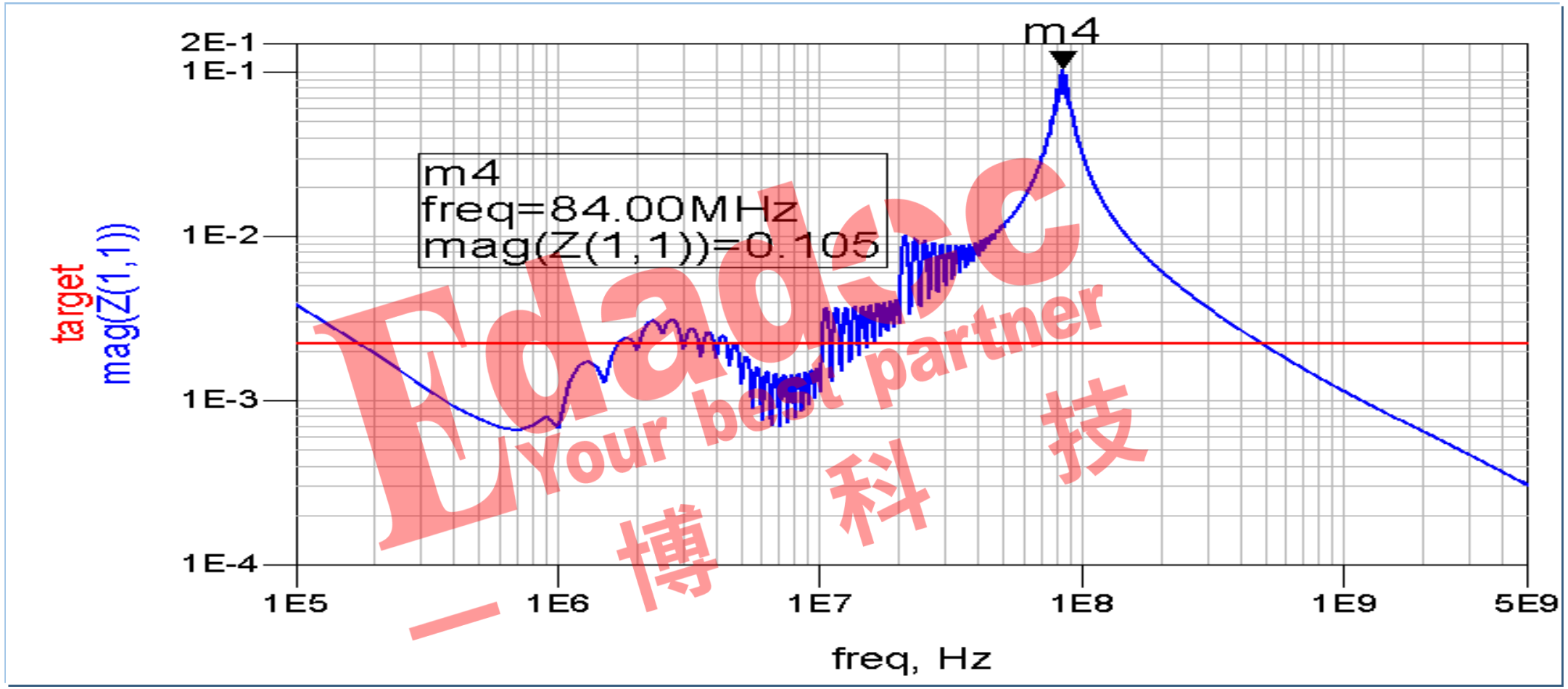
原始设计仿真结果

- 原始全通道PDN结果如下：



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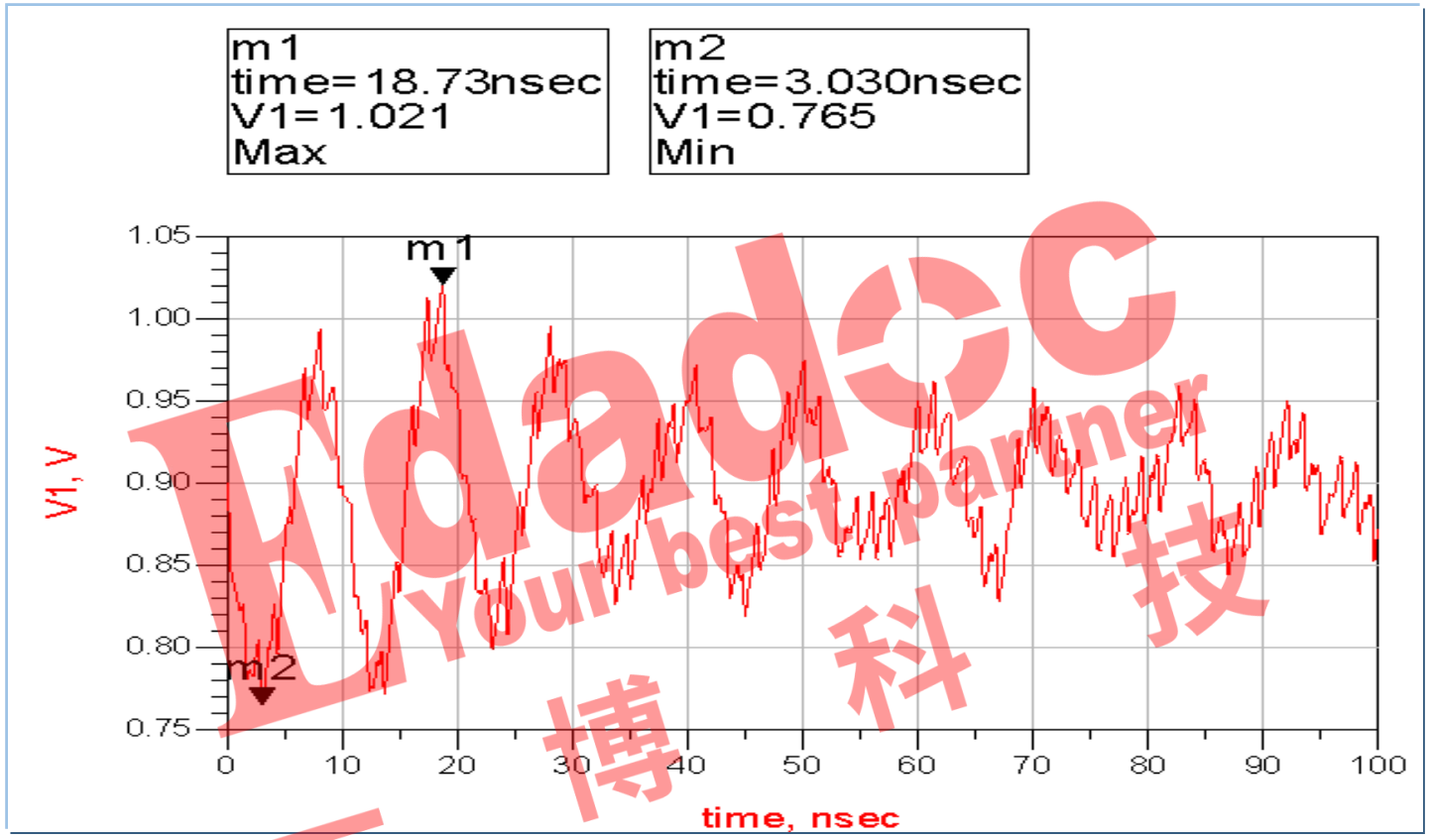
原始设计仿真结果

峰峰值256mV



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希望从PCB板级去改善

- 对该版本的PCB进行电容优化，优化方案如下：

① 从0.47 μF中选出16个改成1 μF

② 封装不变，剩下的0.47 μF变成4.7 μF

③ 其他配置的电容不变

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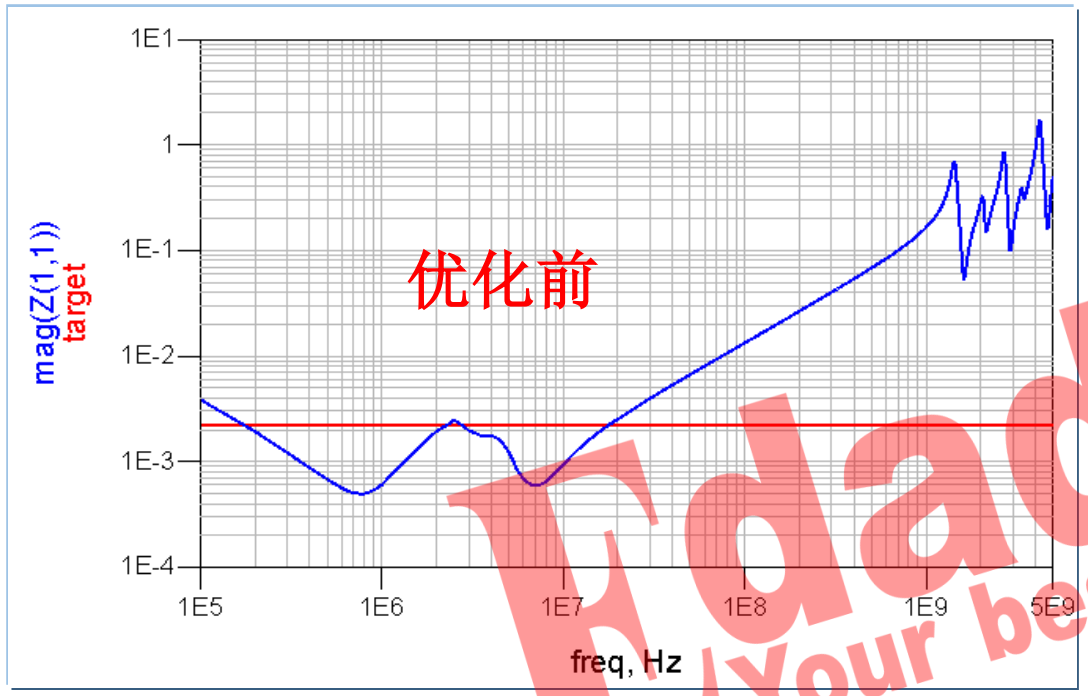
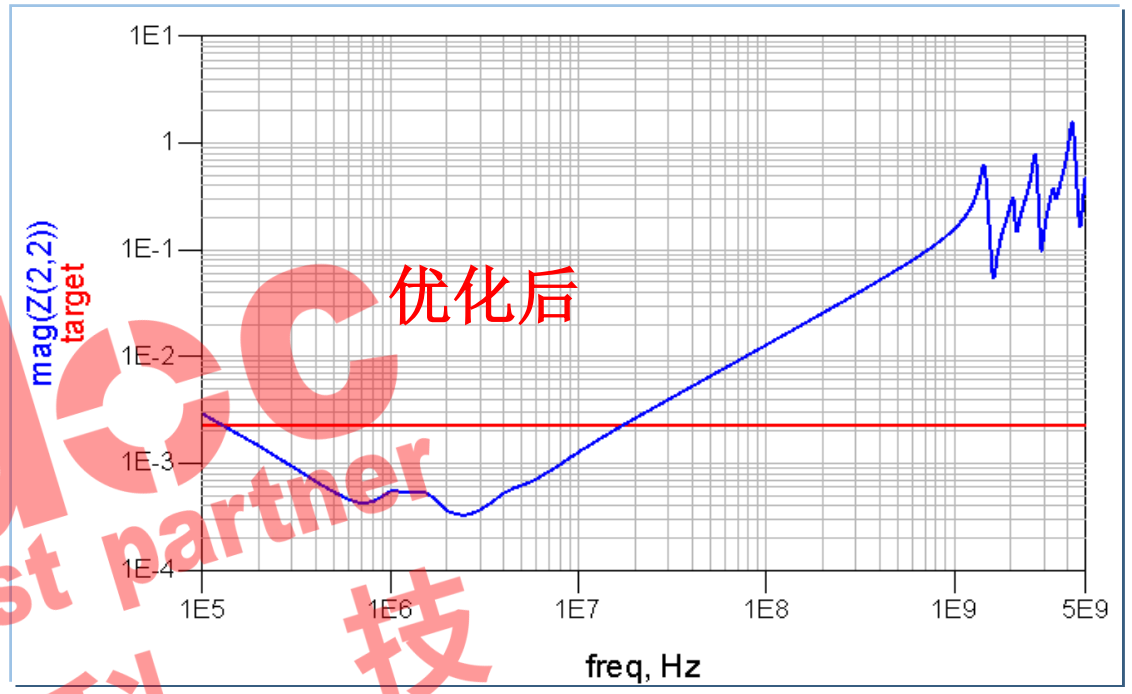
希望从PCB板级去改善





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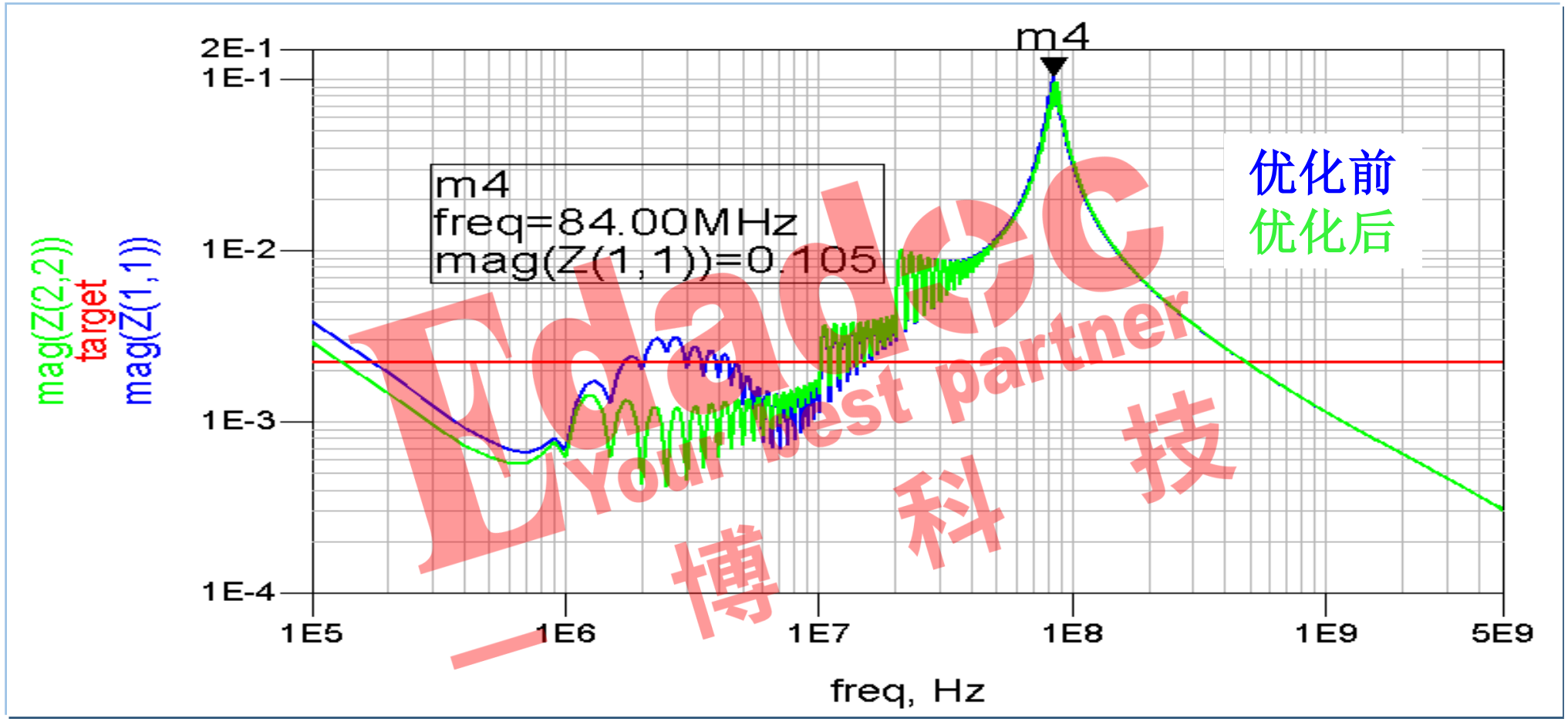
希望从PCB板级去改善

- 优化前后的全通道PDN阻抗对比



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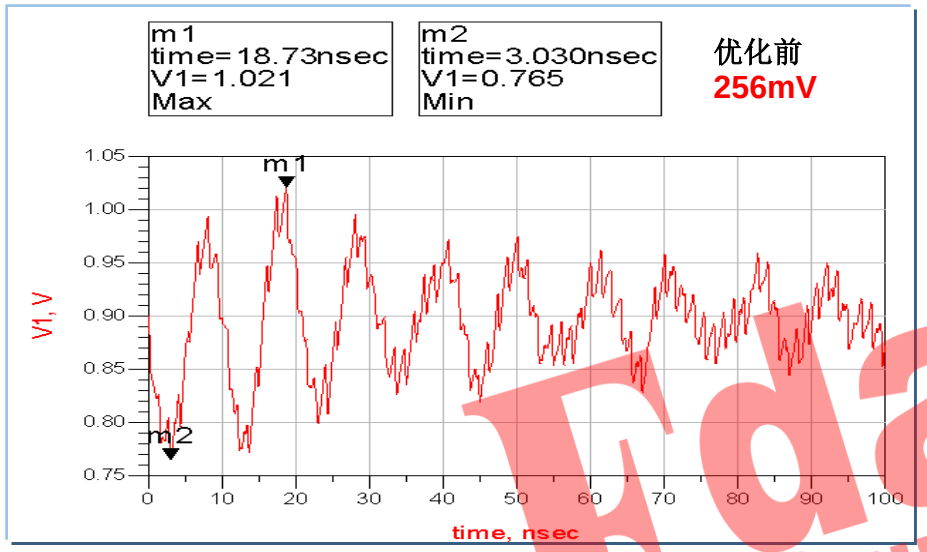
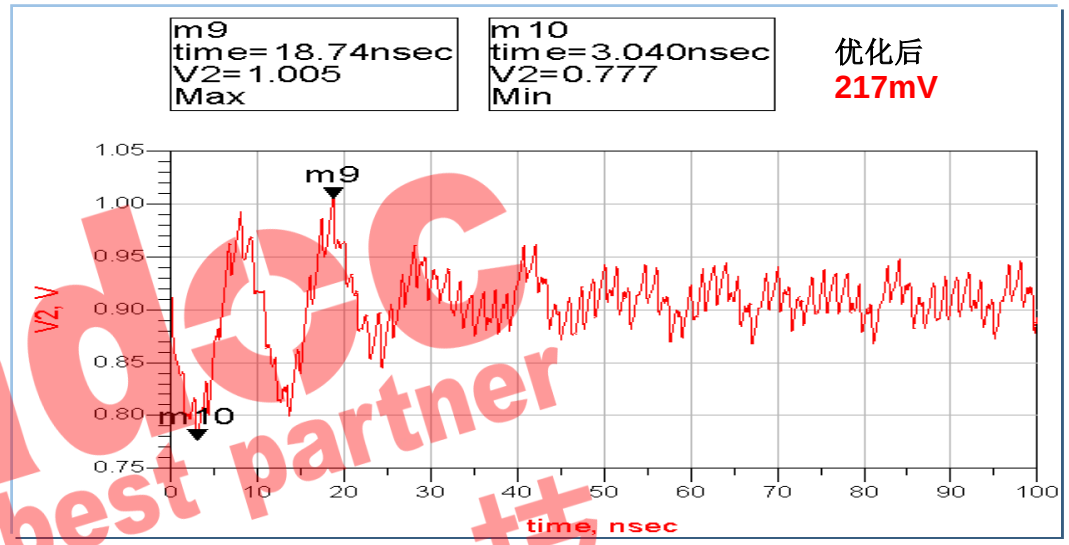
希望从PCB板级去改善

- 电源纹波的改善





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能不能再从PCB板级进一步优化呢

- 重新进行PCB的设计，改为盘中孔和选择0201电容。
- 在第二版PCB基础上，优化方案如下：

① 从0.22 μF中选出12个改成4.7 μF，封装不变

② 从1 μF中选出12个改成4.7 μF，封装不变

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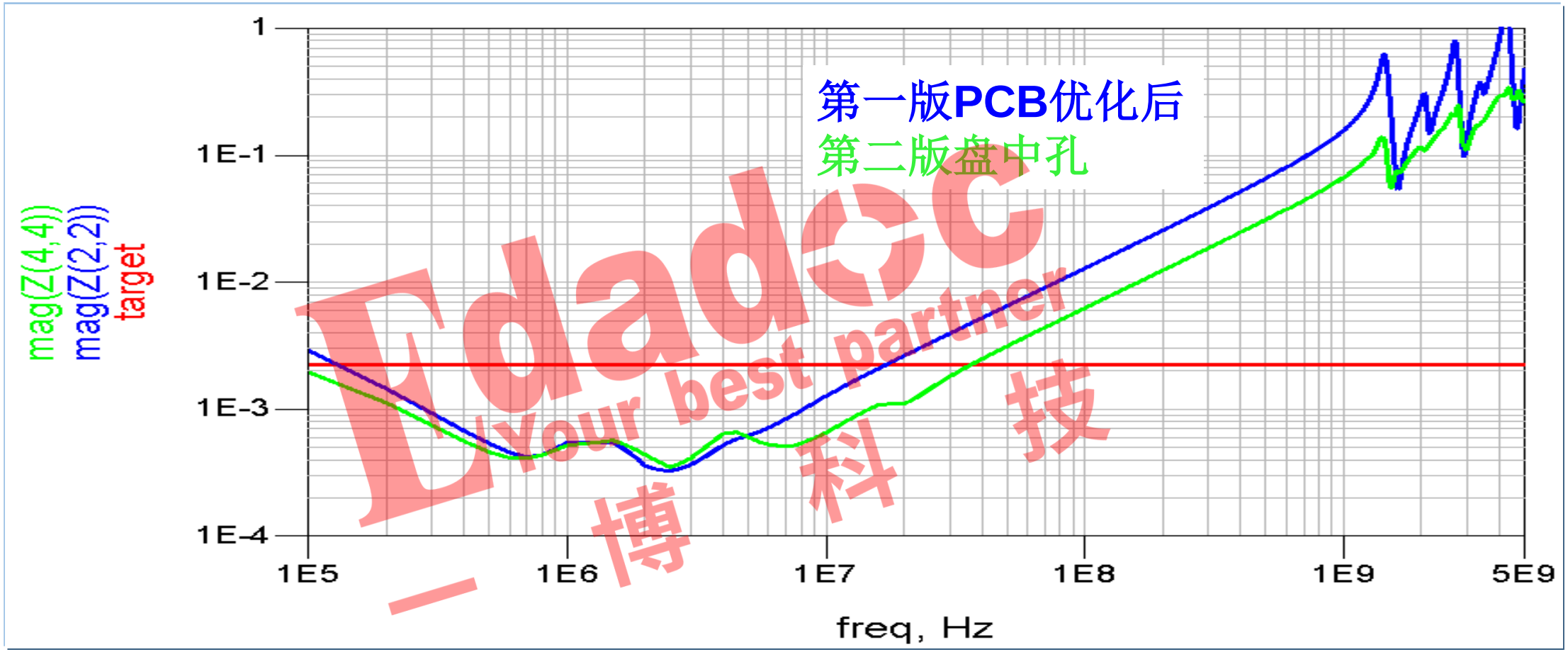
盘中孔加0201电容方案

- 与第一版优化后的板级PDN阻抗对比



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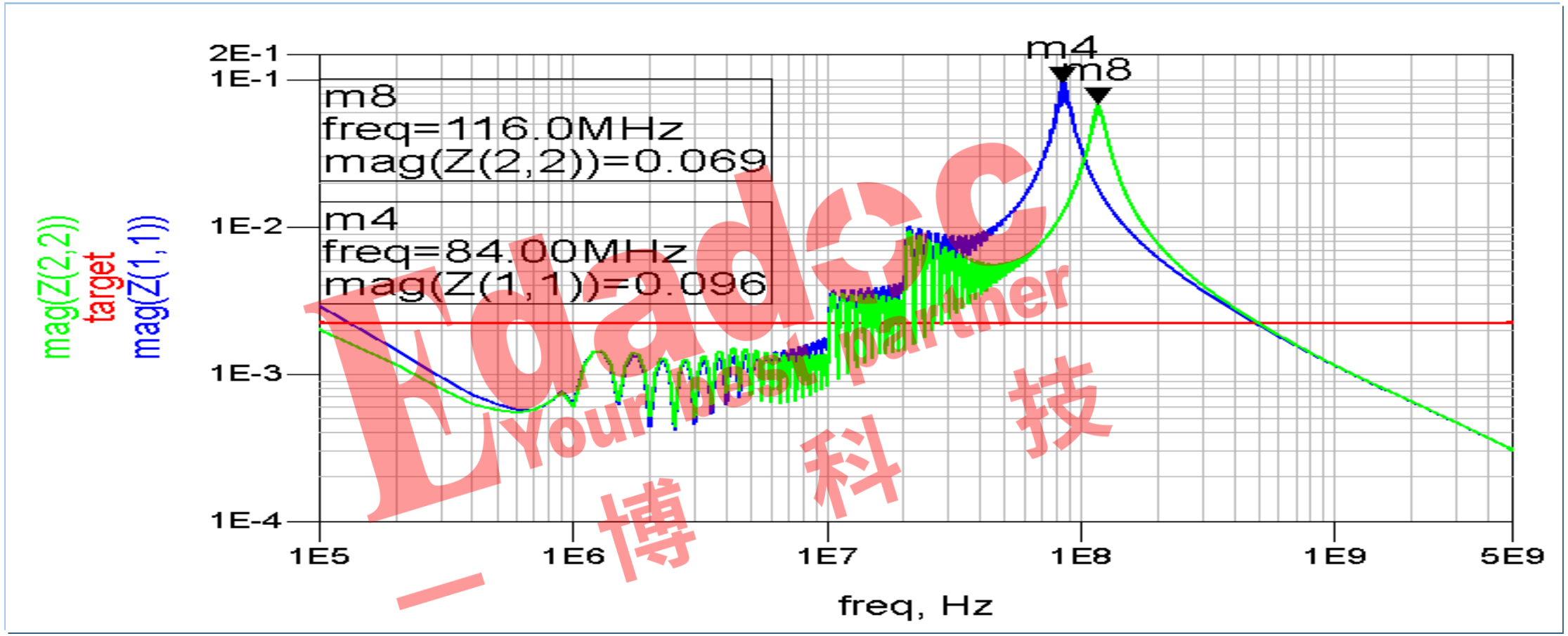
盘中孔加0201电容方案

- 与第一版优化后的全通道PDN阻抗对比



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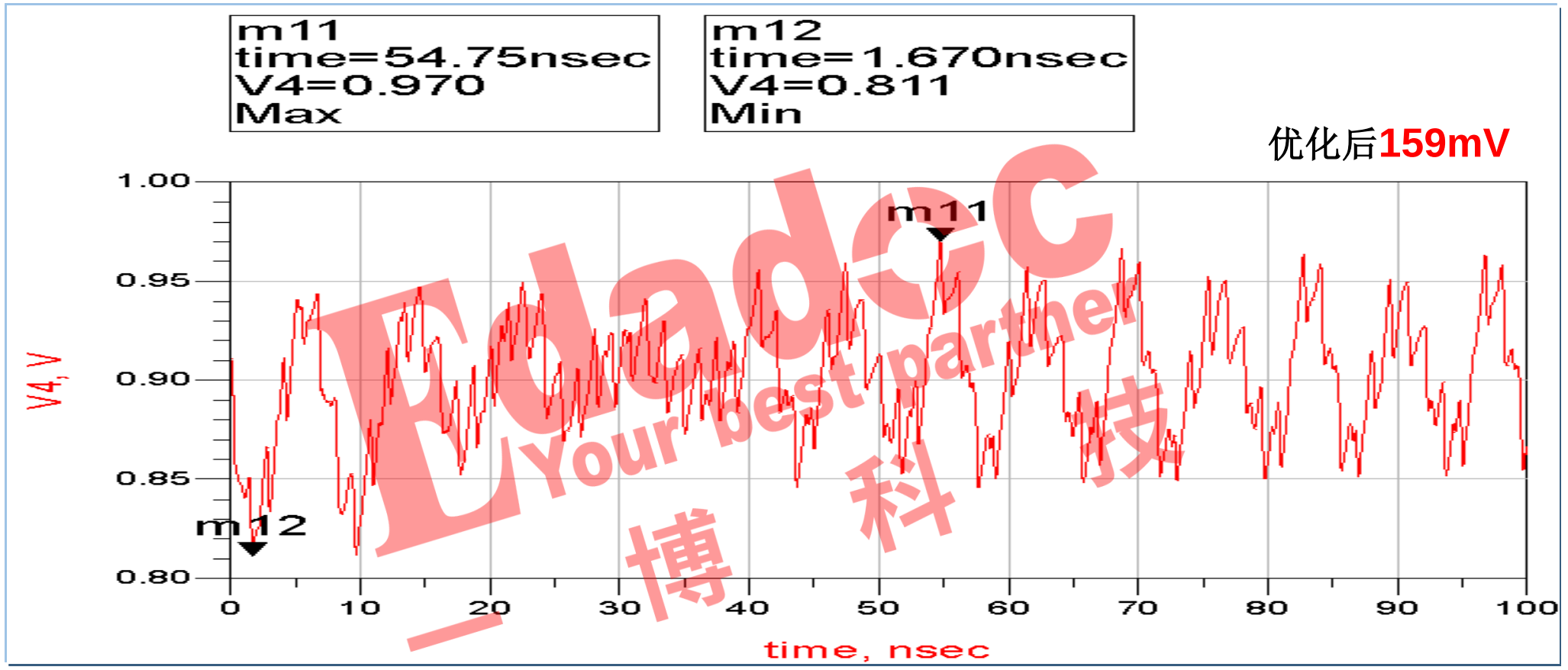
盘中孔加0201电容方案

- 那么电源纹波能改善多少呢?



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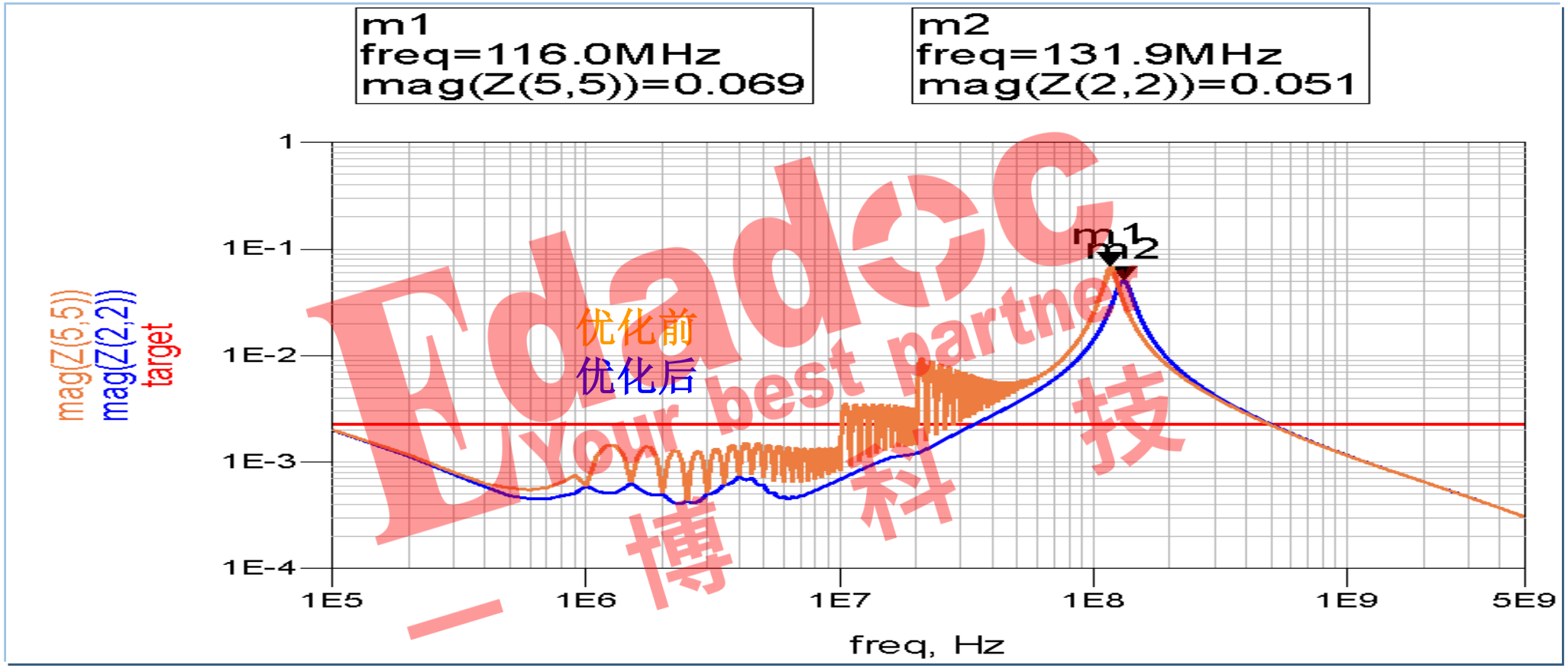
封装基板的优化

- 方案一的全链路PDN阻抗如下：



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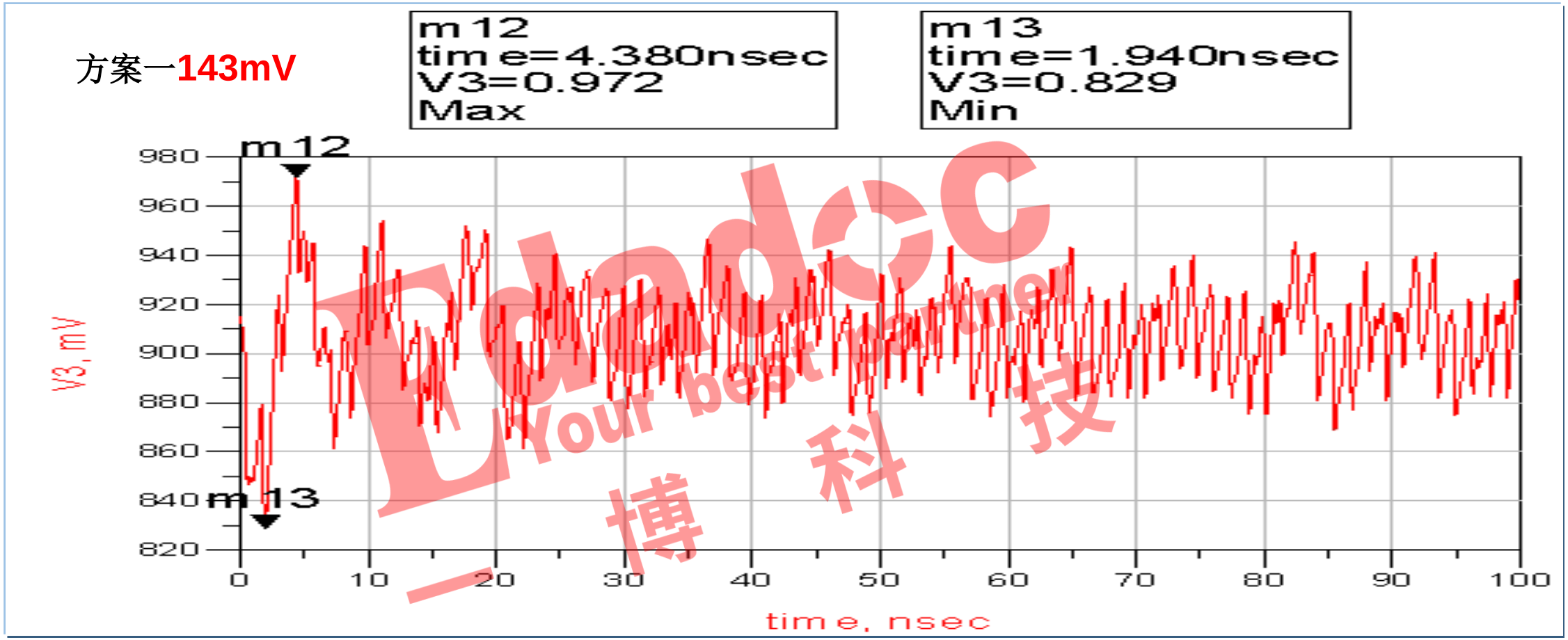
封装基板的优化

- 方案一的全链路电源纹波如下：



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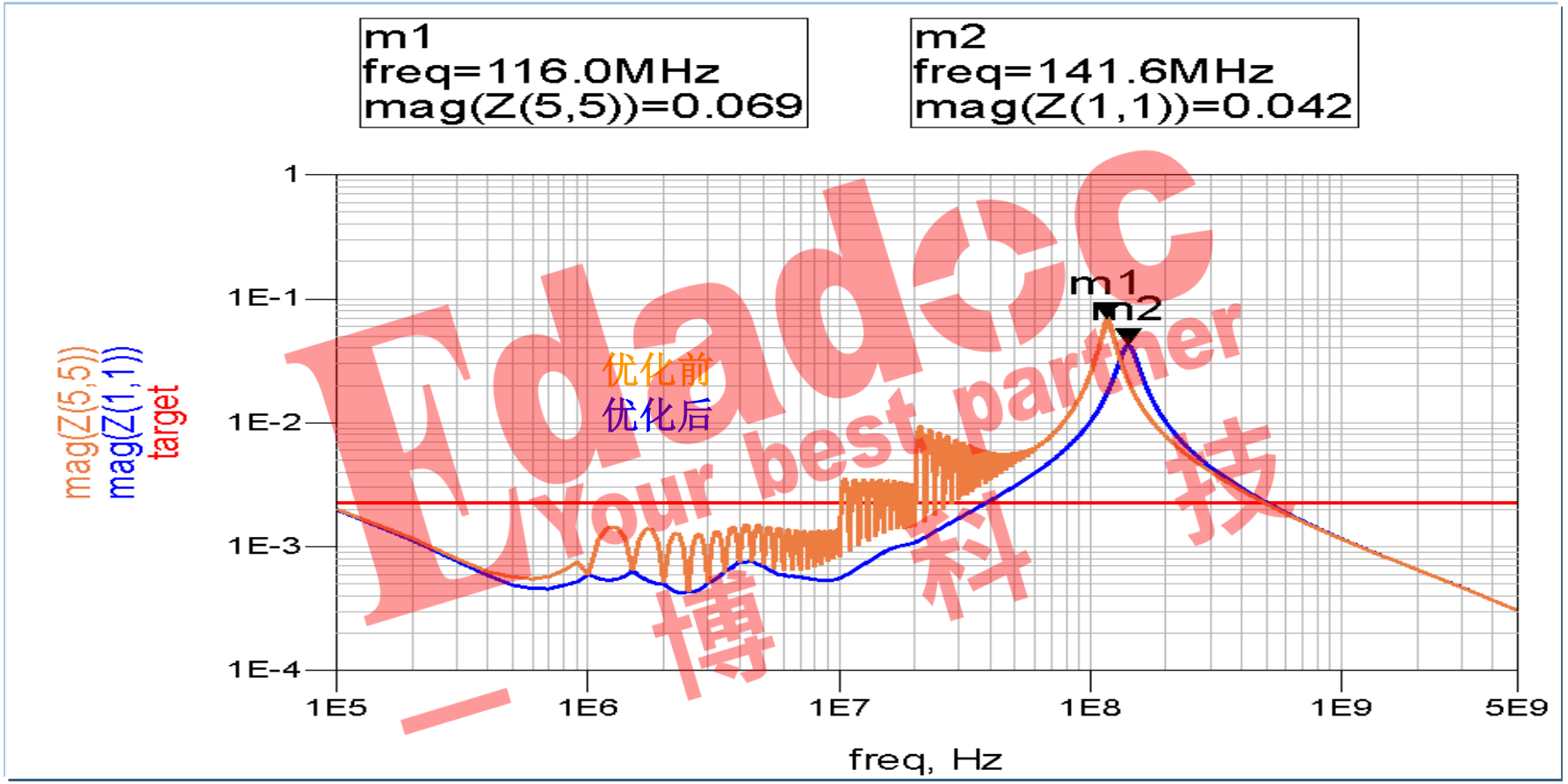
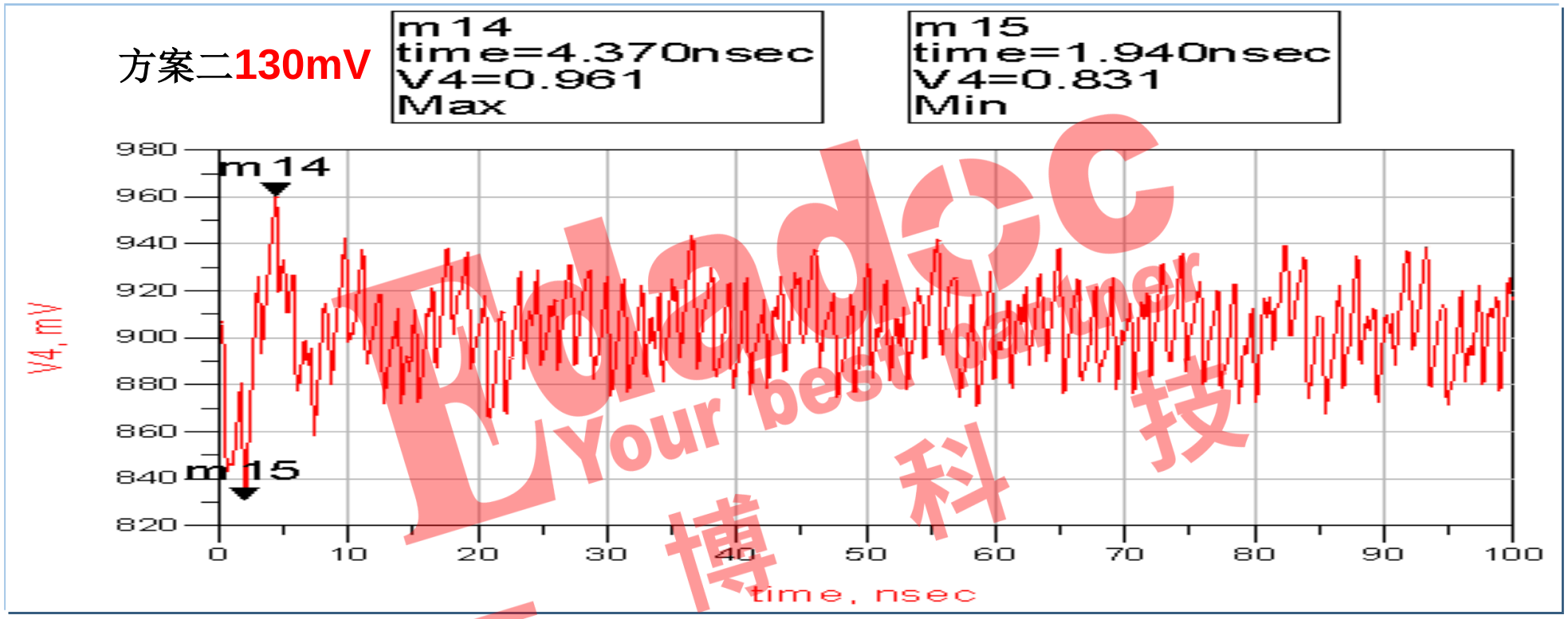
封装基板的优化

- 方案二的全链路PDN阻抗如下：



封装基板的优化

- 方案二的全链路电源纹波如下：



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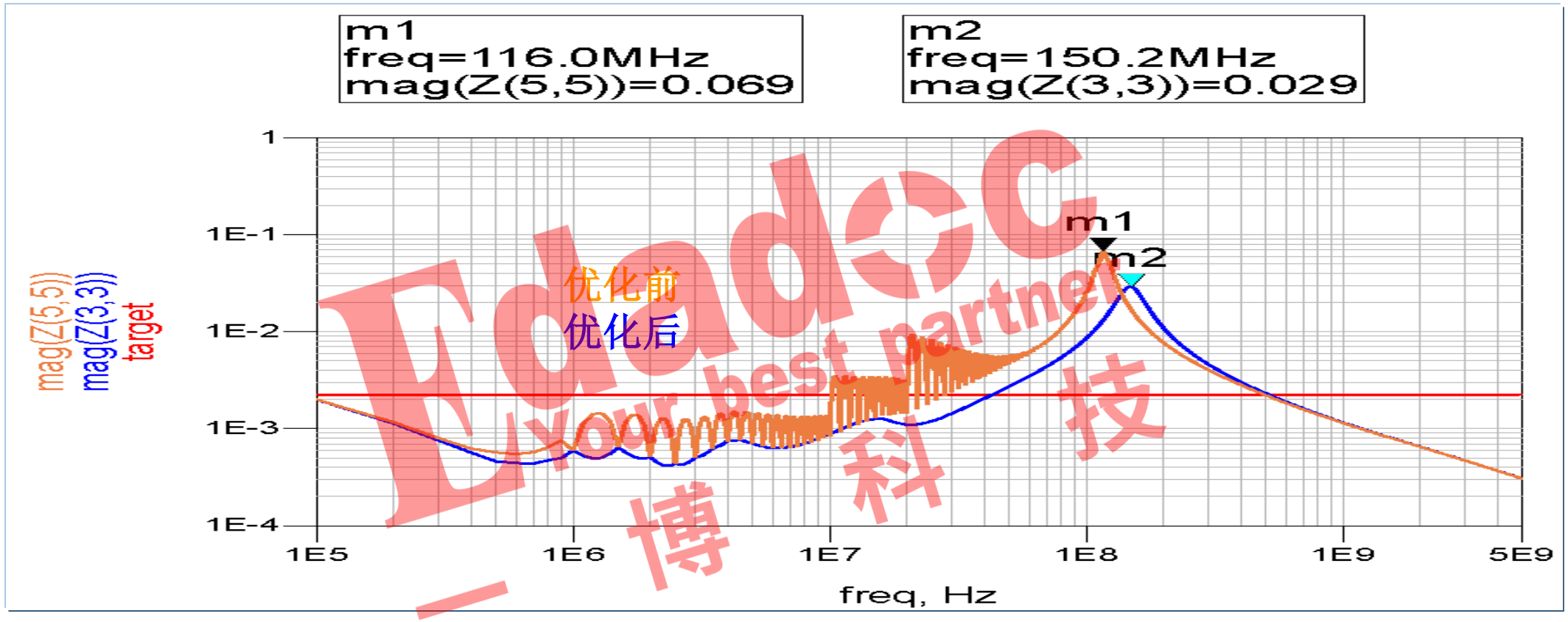
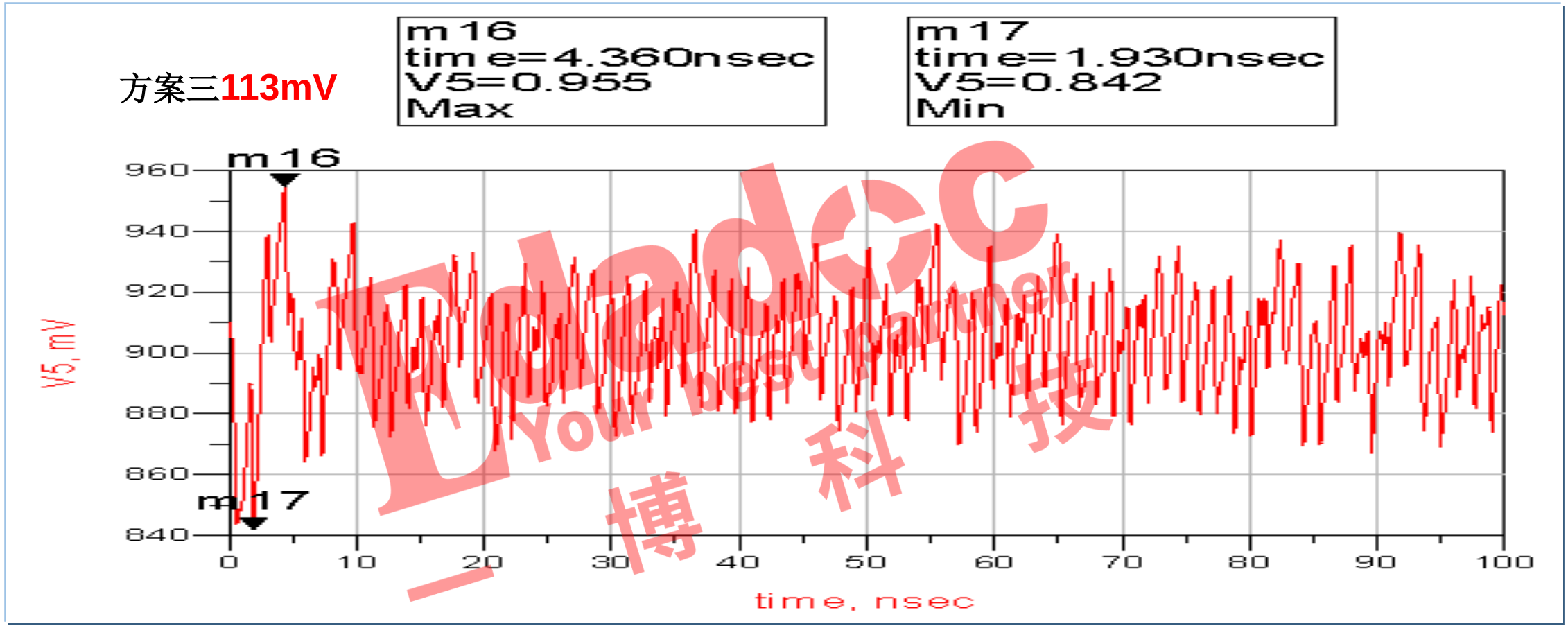
封装基板的优化

- 方案三的全链路PDN阻抗如下：



封装基板的优化

- 方案三的全链路电源纹波如下：



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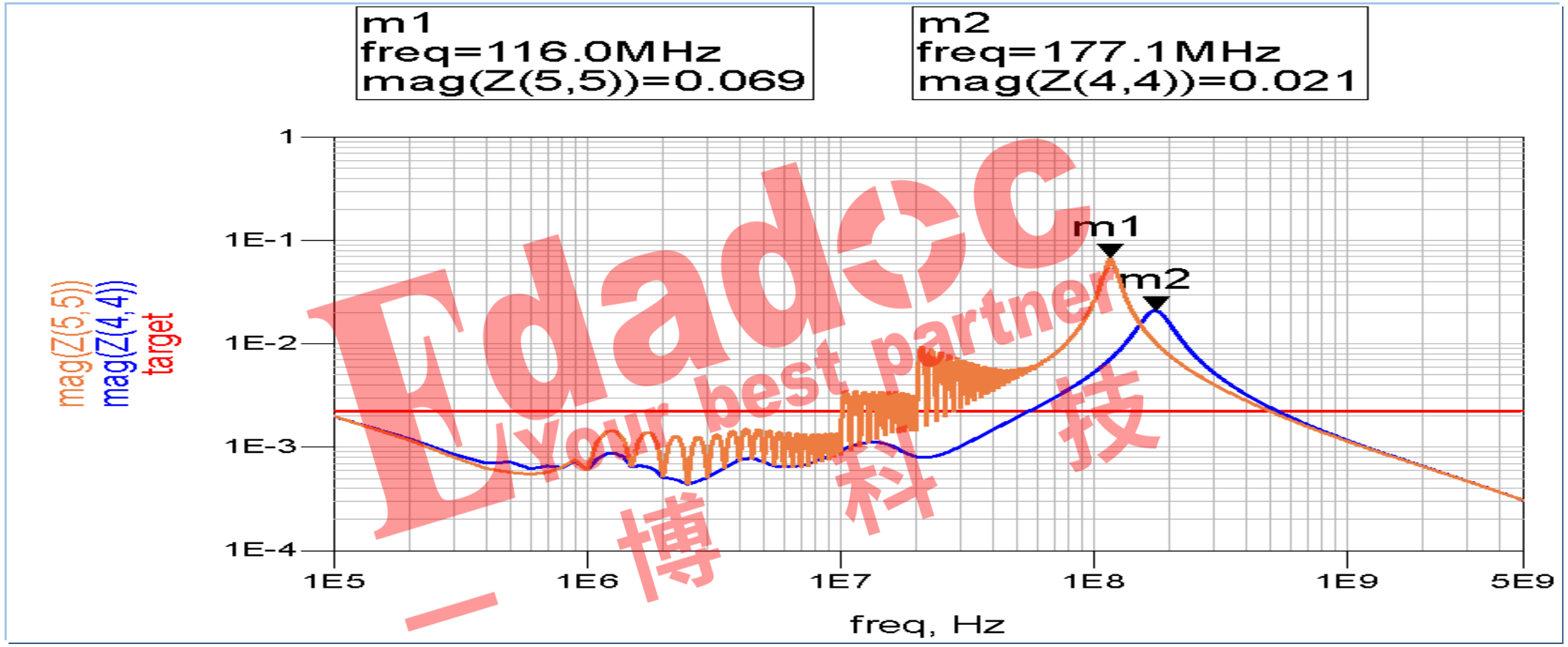
封装基板的优化

- 方案四的全链路PDN阻抗如下：



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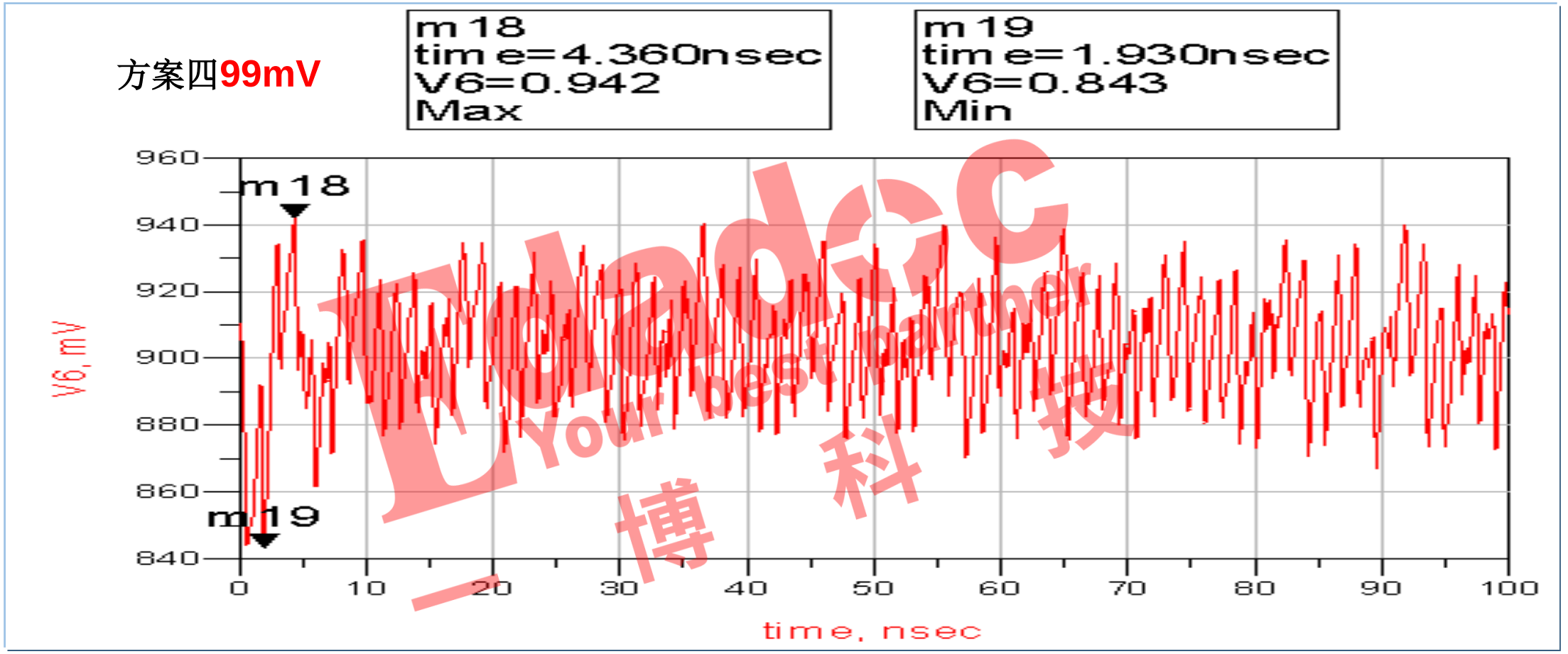
封装基板的优化

- 方案四的全链路电源纹波如下：



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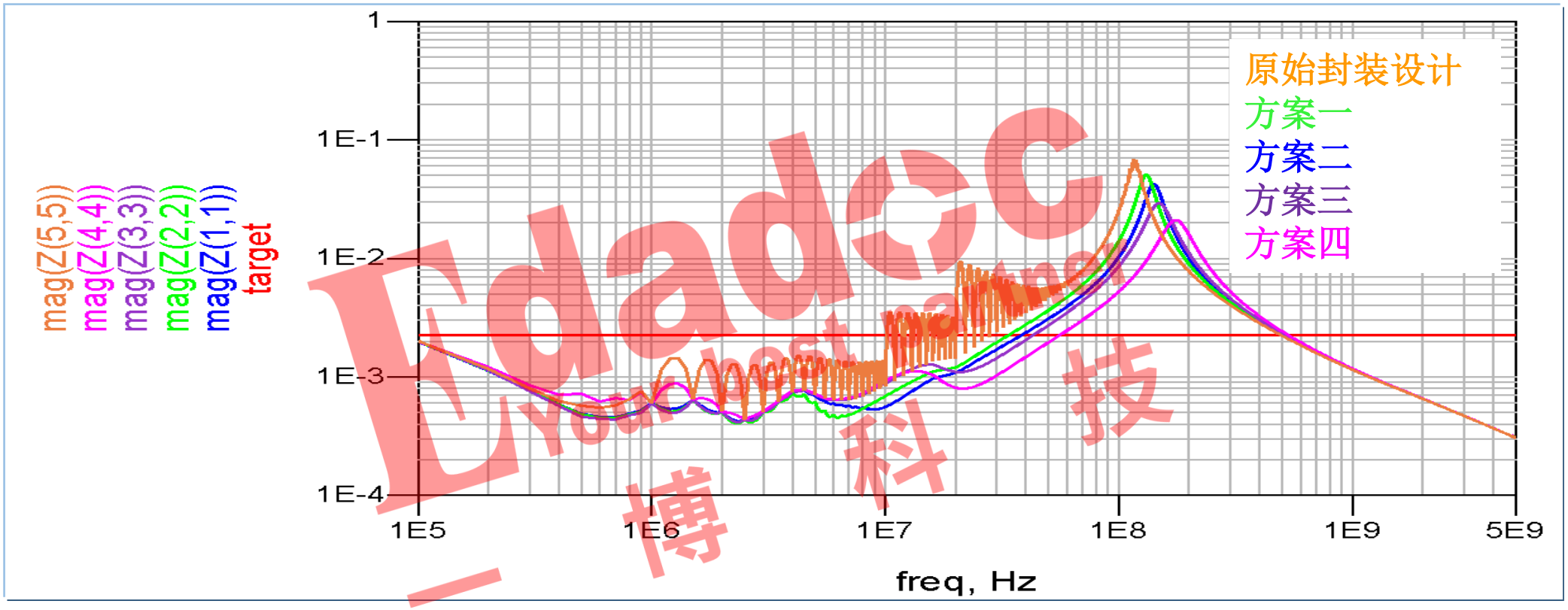
封装基板的优化

- 几个方案的PDN阻抗汇总



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Part 05

总结

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PDN阻抗仿真的意义

- 目标阻抗法可以快速评估PDN系统的阻抗是否满足要求；
- 目标阻抗值及对应频段可通过经验估算，更精确的是参考芯片手册的电源要求；
- PDN阻抗仿真可实现对电容的配置（容值组合、数量）与电容Layout的指导；
- 全链路PDN阻抗优化，需要协同板级电源设计、封装电源设计以及片上电容三部分。

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THANK YOU!

谢谢观看！

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