

信号完整性测试

你的产品质检员

—博科技-SI研究部

EDADOC, Your Best Partner



产品出来后怎么判断产品性能，忐忑出货/底气十足？

- 只做功能性测试？
 - 长时间
 - 高低温
- 两条腿走路？——功能性测试+ 信号完整性测试同时进行
 - 波形/眼图
 - 时序
 - 轻载/重载



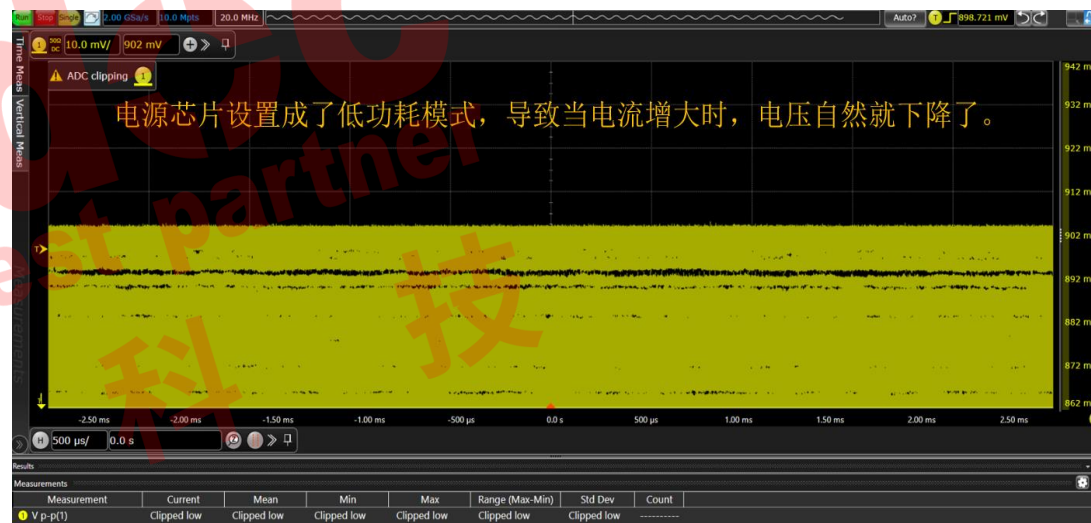
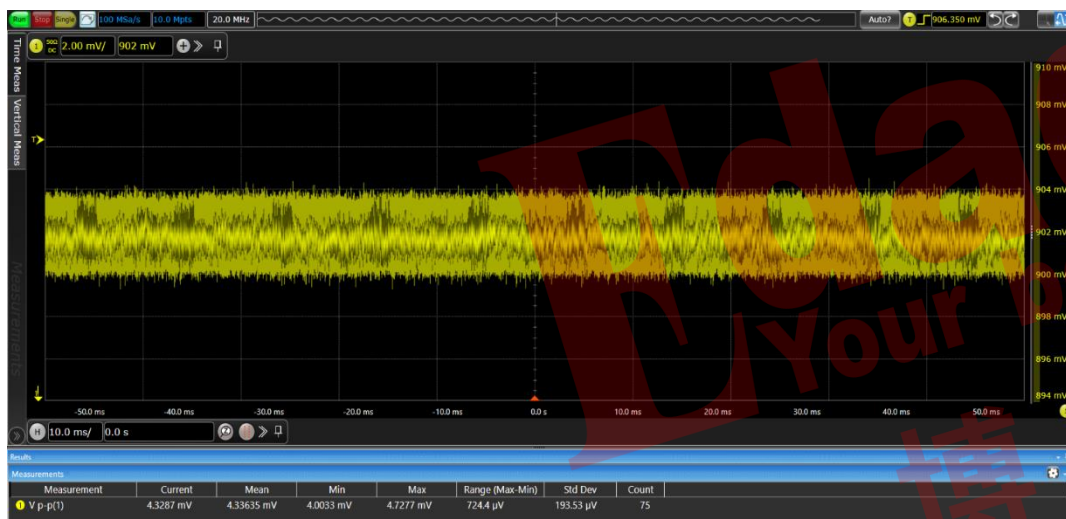
PART 01

什么时候你想SI测试了



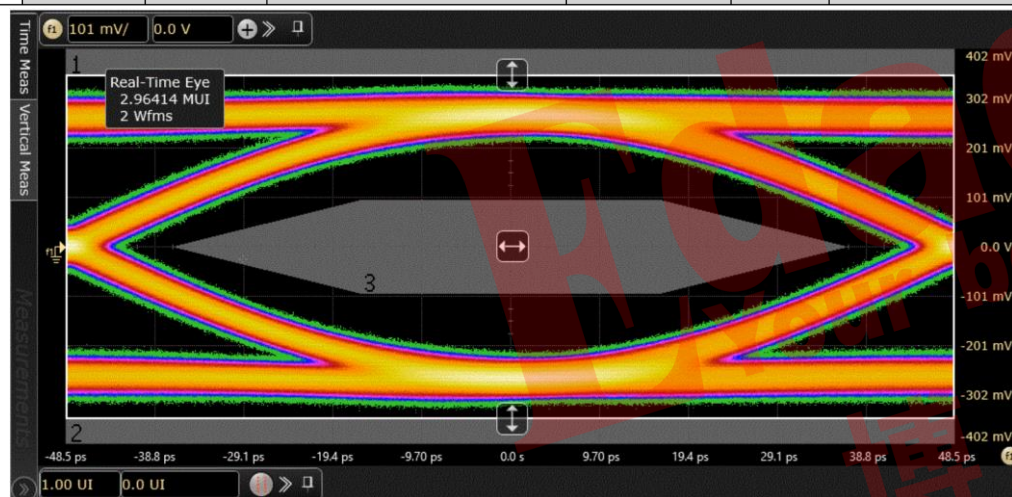
客户：对业务端口初始化，温度升高一会儿就挂了，少初始化一些端口就能够建链。业务端口起来的越多，功耗越高，怀疑是纹波过大造成的

- 芯片上电——系统正常，且纹波 $\leq 5\text{mVpp}$
- 所有业务端口初始化起来——系统挂了，电压明显下降，从0.9V降到了0.85V，且不会回到0.9V

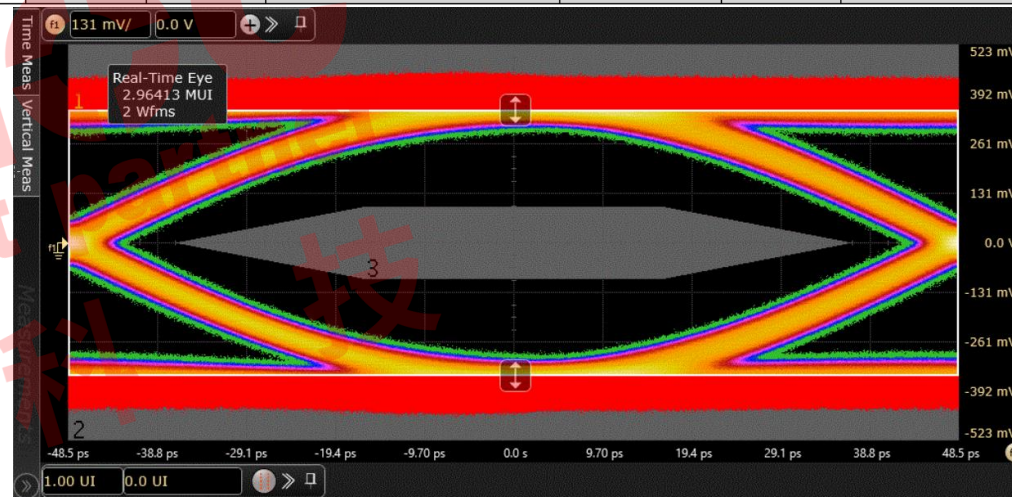


- 产品发货两年了，功能没问题，从没测过眼图；现在的客户要求必须见到SI测试报告
- 幅度过大有什么影响？

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	Total Jitter (TJ)(p-p)	182.4 mUI	34.9	VALUE <= 280.0 mUI
✓	0	1	Eye Mask Hit Ratio	0.0000000	100.0	VALUE <= 50.0 μ

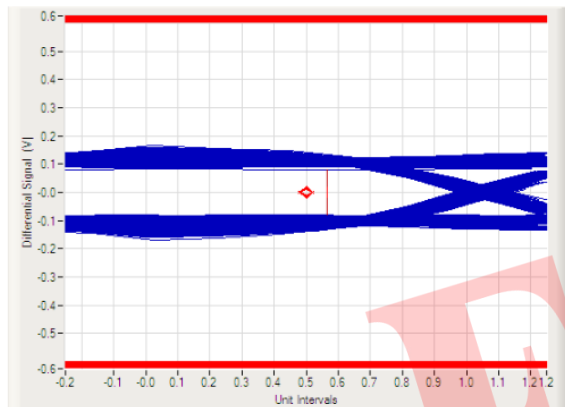


Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	Total Jitter (TJ)(p-p)	184.6 mUI	34.1	VALUE <= 280.0 mUI
✗	1	1	Eye Mask Hit Ratio	459.1975 m	-918E+03	VALUE <= 50.0 μ

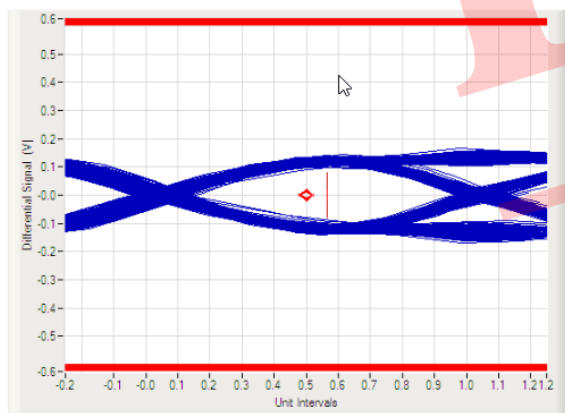


- 无法限制客户使用特定的板卡，只能让自己调整到最优，以补他人之短

Worst Non Transition Signal Eye



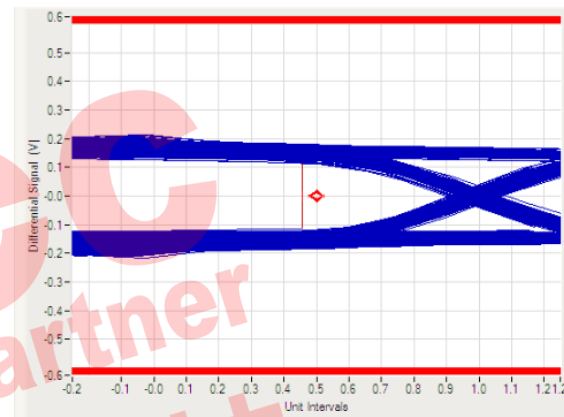
Worst Transition Signal Eye



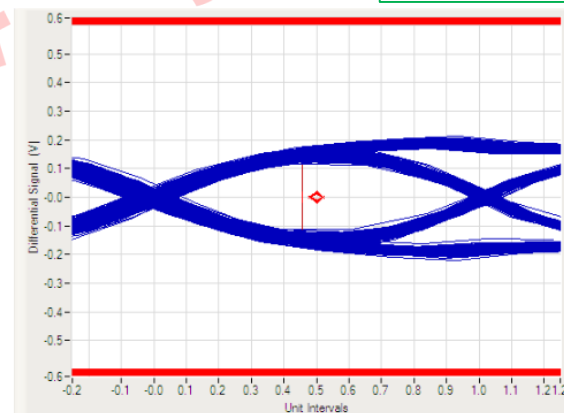
● Overall Sigtest Result: **Pass!**

挑出最好的preset

Worst Non Transition Signal Eye

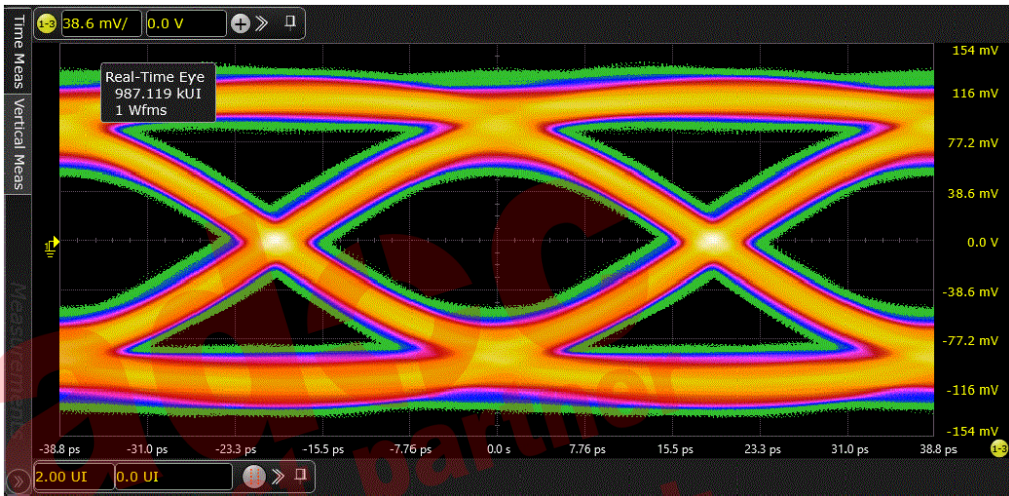


Worst Transition Signal Eye



● Overall Sigtest Result: **Pass!**

- 按照芯片推荐的值，眼图虽PASS，但裕量≈没有



Summary of Results

Test Statistics	
Failed	0
Passed	4
Total	4

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	Signaling Rate	25.781508000 Gbps	45.0	25.778671875 Gbps <= VALUE <= 25.783828125 Gbps
✓	0	1	Eye Height A	95.00 m	0.0	VALUE >= 95.00 m
✓	0	1	Eye Width	729.69 m	58.6	VALUE >= 460.00 m
✓	0	1	Eye Height B	93.10 m	16.4	VALUE >= 80.00 m

- 有病治病，无病防身
——第一时间发现问题，解决问题，防微杜渐



PART 02

DDR测试



- 波形质量：幅度、斜率、占空比、过冲
- 时序：建立/保持时间
- 眼图

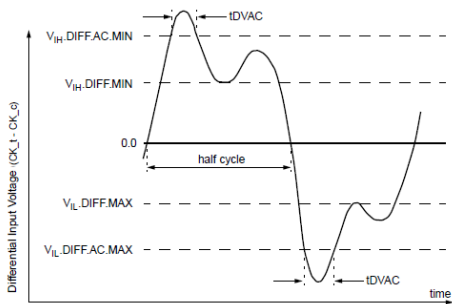


Figure 2. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	differential input high	+0.150	NOTE 3	+0.135	NOTE 3	+0.135	NOTE 3	+0.125	NOTE 3	TBD	NOTE 3	V	1
V _{IL}	differential input low	NOTE 3	-0.150	NOTE 3	-0.135	NOTE 3	-0.135	NOTE 3	-0.125	NOTE 3	TBD	V	1
V _{OH} (AC)	differential input high ac	2 × (V _{OH} (AC) - V _{REF})		2 × (V _{OH} (AC) - V _{REF})		2 × (V _{OH} (AC) - V _{REF})		2 × (V _{OH} (AC) - V _{REF})		2 × (V _{OH} (AC) - V _{REF})		V	2
V _{OL} (AC)	differential input low ac	2 × (V _{OL} (AC) - V _{REF})		2 × (V _{OL} (AC) - V _{REF})		2 × (V _{OL} (AC) - V _{REF})		2 × (V _{OL} (AC) - V _{REF})		2 × (V _{OL} (AC) - V _{REF})		V	2

8.7 AC and DC Logic Input Levels for DQS Signals

8.7.1 Differential signal definition

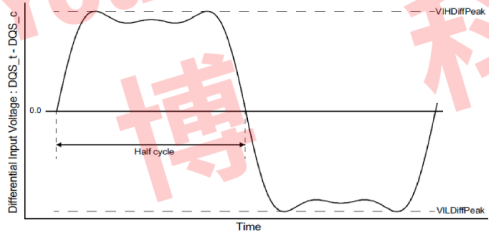


Figure 11. Definition of differential DQS signal AC-swing level

8.7.2 Differential swing requirements for DQS (DQS_t - DQS_c)

[Table 17] Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH} DiffPeak	V _{IH} DIFF Peak Voltage	186	Note2	160	Note2	150	Note2	145	Note2	140	Note2	mV	1
V _{IL} DiffPeak	V _{IL} DIFF Peak Voltage	Note2	-186	Note2	-160	Note2	-150	Note2	-145	Note2	-140	mV	1

NOTE:
1) Used to define a differential signal slew-rate.
2) These values are not defined, however, the differential signals DQS_i - DQS_j, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

[Table 57] Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
tIS(base, AC100)	115	100	80	62	-	-	-	ps	VIHL(ac)
tIH(base, DC75)	140	125	105	87	-	-	-	ps	VIHL(dc)
tIS(base, AC 90)	-	-	-	-	55	48	40	ps	VIHL(ac)
tIH(base, DC 65)	-	-	-	-	80	73	65	ps	VIHL(dc)
tIS/tIH @ VREF	215	200	180	162	145	138	130	ps	

NOTE:
1) Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.
2) Values listed are referenced only; applicable limits are defined elsewhere.

[Table 58] Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
V _{IH} .CA(AC)min	100	100	100	100	90	90	90	mV	VIHL(ac)
V _{IH} .CA(DC)min	75	75	75	75	65	65	65	mV	VIHL(dc)
V _{IL} .CA(DC)max	-75	-75	-75	-75	-65	-65	-65	mV	VIHL(dc)
V _{IL} .CA(AC)max	-100	-100	-100	-100	-90	-90	-90	mV	VIHL(ac)

NOTE:
1) Command, Address, Control input levels relative to VREFCA.
2) Values listed are referenced only; applicable limits are defined elsewhere.

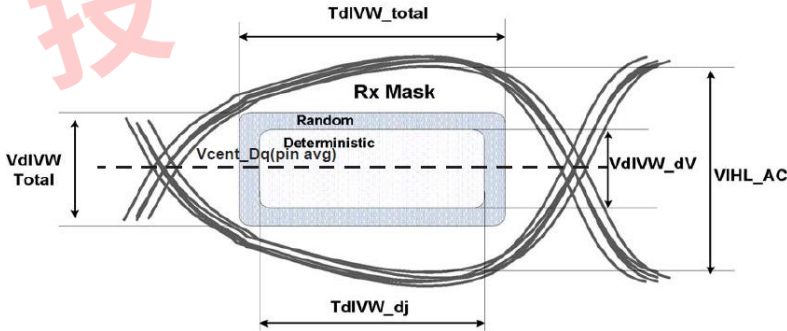
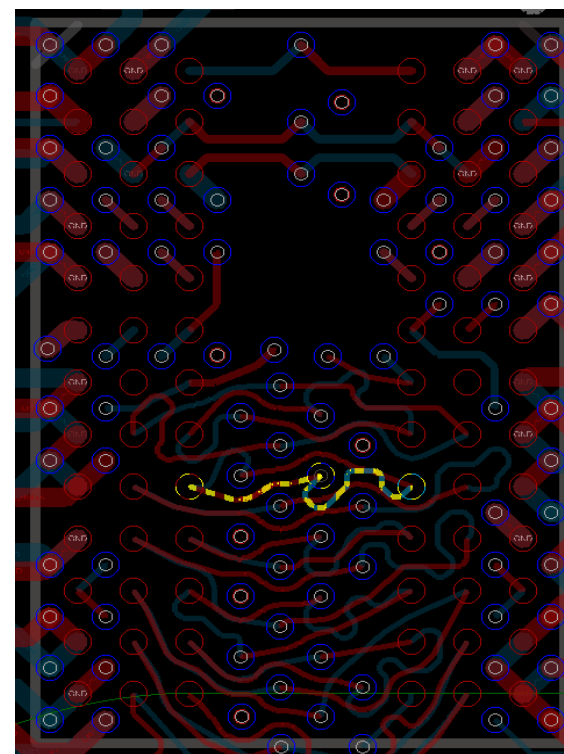
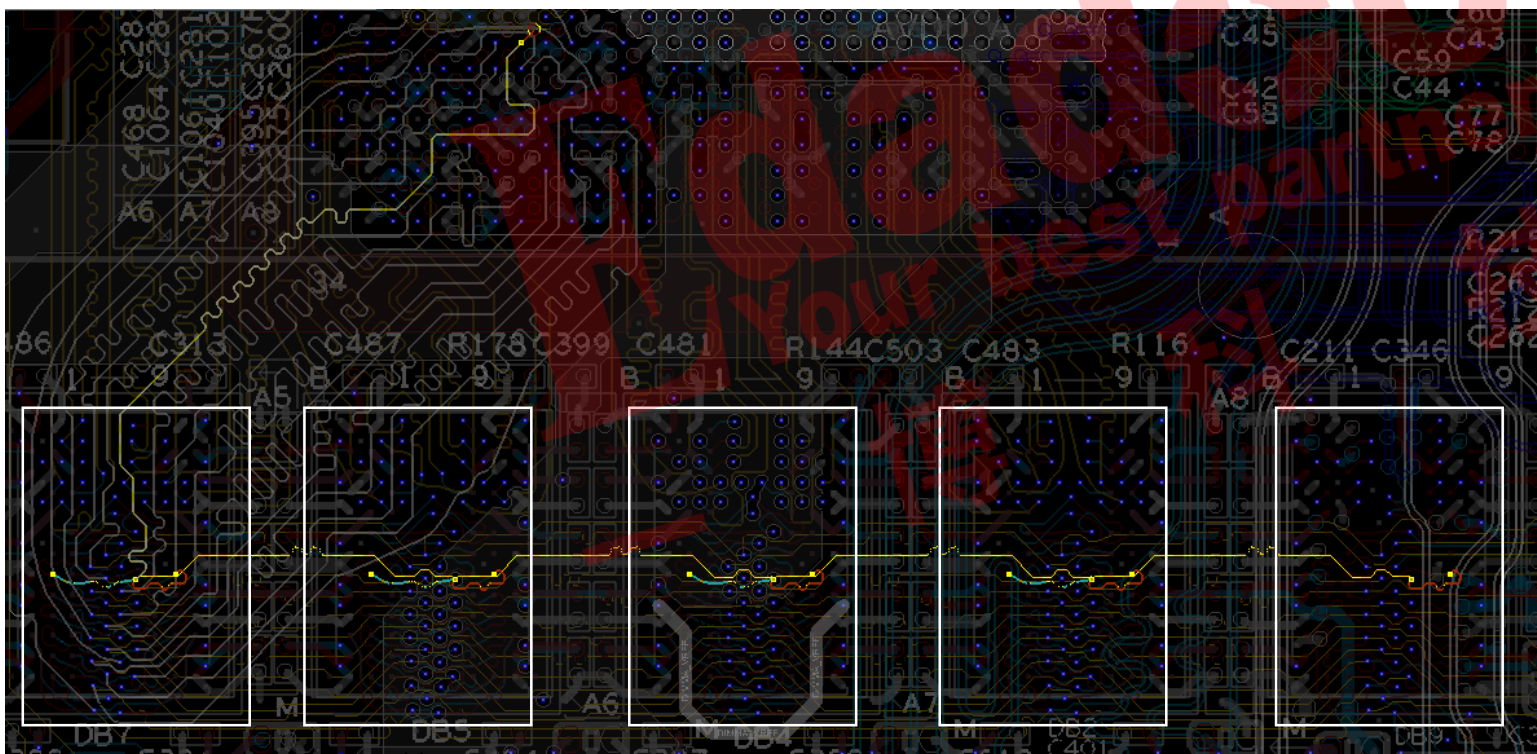


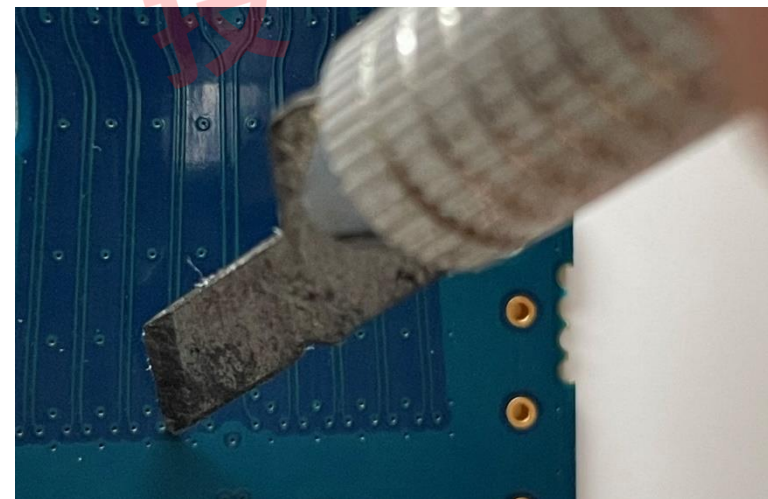
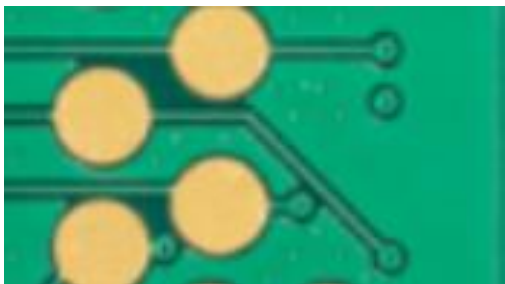
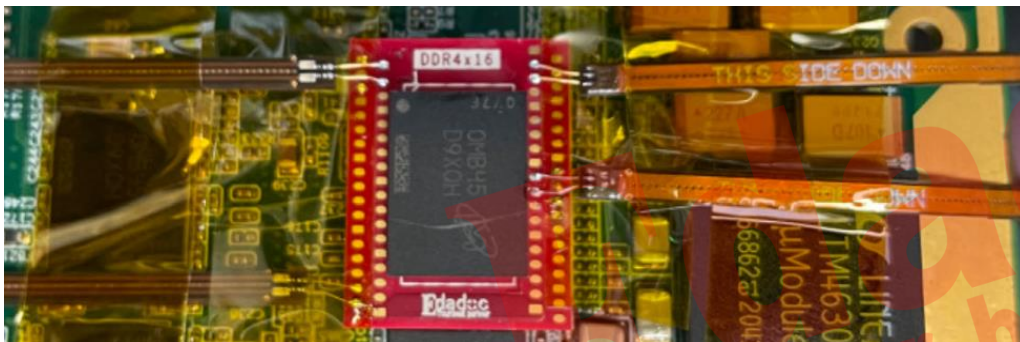
Figure 186 — DQ Receiver(Rx) compliance mask

Symbol	Parameter	1600/1866/2133		2400	2666	2933	3200	Unit	NOTE
		min	max	min	max	min	max		
VdIVW	Rx Mask voltage - pk-pk	-	136	-	130	-	115	mV	1,2,10
TdIVW	Rx timing window	-	0.2	-	0.22	-	0.23	UI*	1,2,10

- 拓扑结构：1拖多，测几颗颗粒？ 每个颗粒测几对网络？
——人工测、人工判决、人工整理数据成报告，工作量大、时间长
- 颗粒正反贴，没有任何测试点
——没法接到示波器，测不了



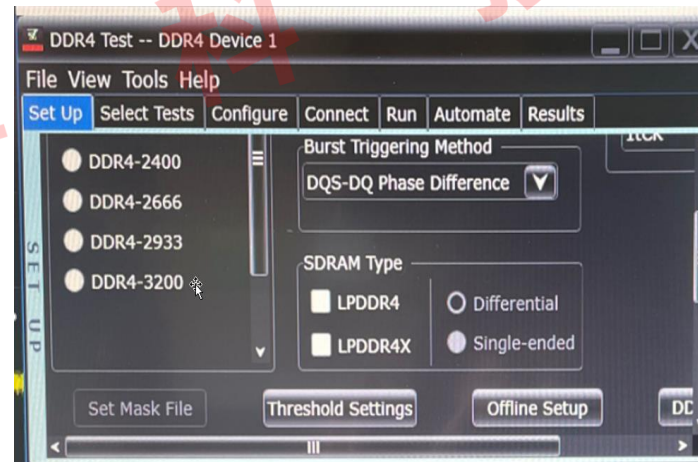
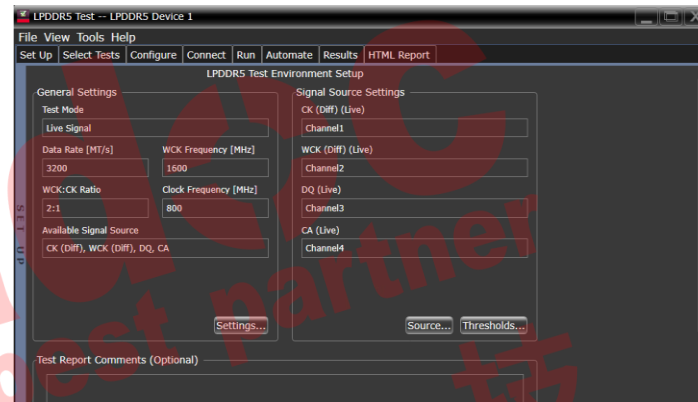
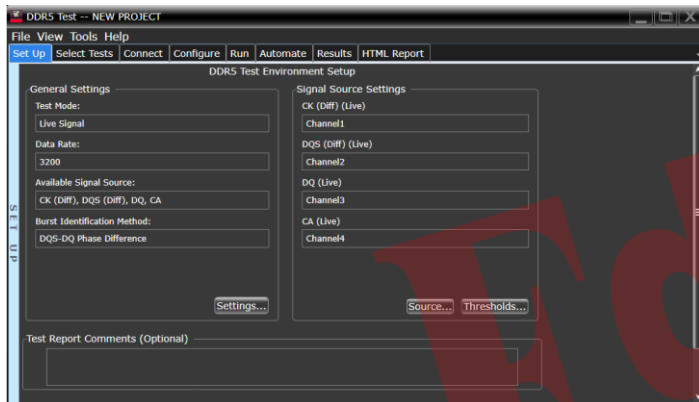
- 留了测试点
- 没留测试点，但有些信号可以刮孔测试
- 无测试点，无孔可刮，怎么办？



- 一致性测试软件：
DDR4/DDR5/LPDDR5
- 自动生成的测试报告



DDR4 5 test
report



PART 03

串行总线测试



无源SPEC——前期评估、仿真

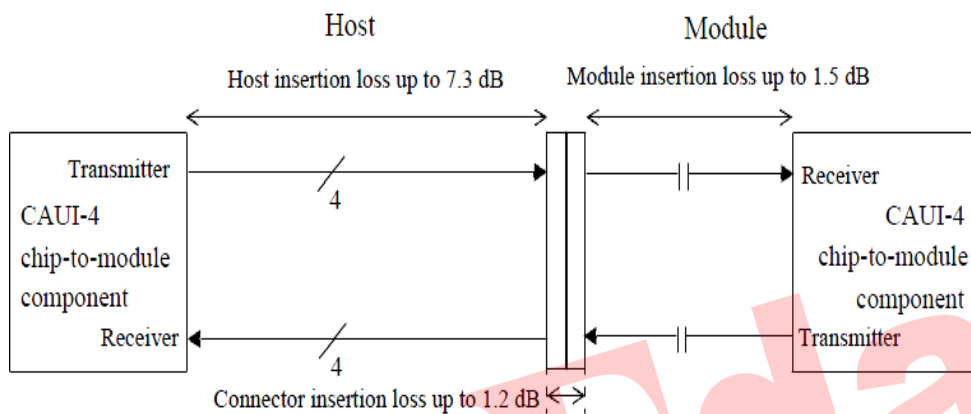
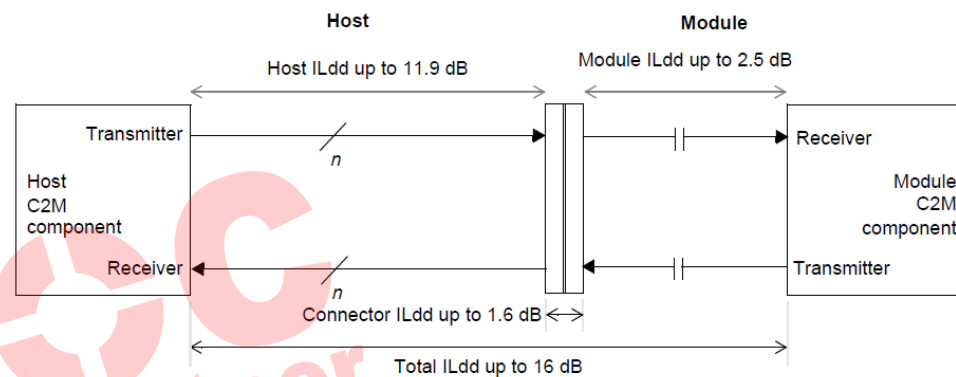


Figure 83E-2—Chip-to-module insertion loss budget at 12.89 GHz



NOTE—The number of lanes n is equal to 1 for 100GAUI-1, 2 for 200GAUI-2, and 4 for 400GAUI-4.

Figure 120G-2—100GAUI-1, 200GAUI-2, and 400GAUI-4 C2M differential-mode to differential-mode insertion loss budget at 26.56 GHz

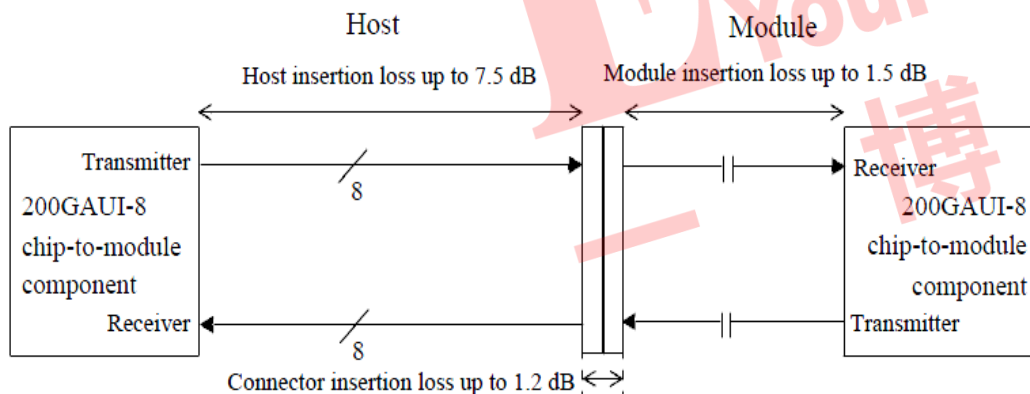


Figure 120C-2—200GAUI-8 chip-to-module insertion loss budget at 13.28 GHz

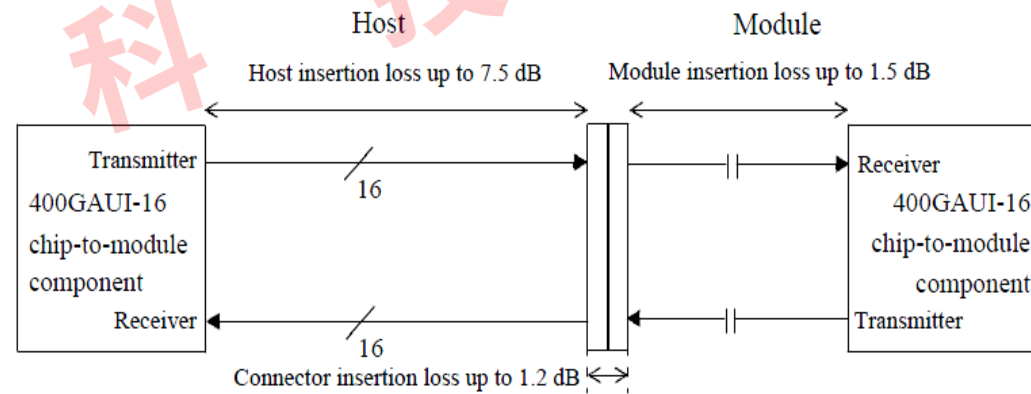
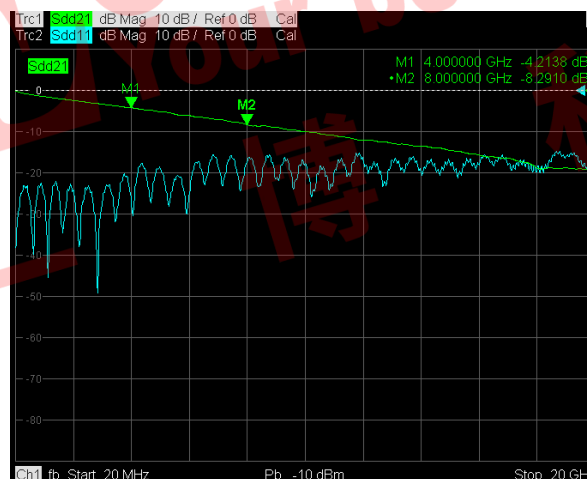
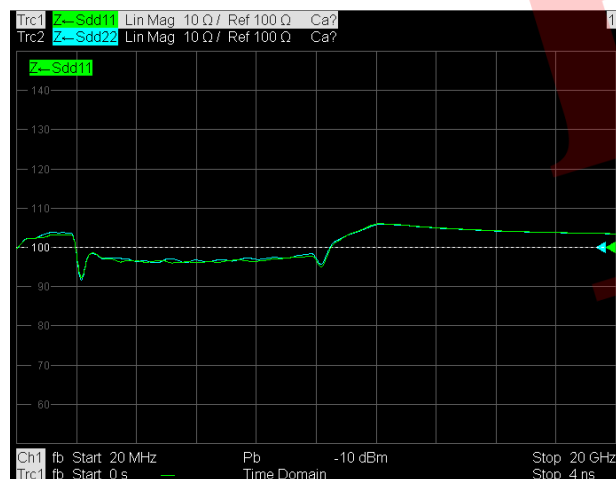
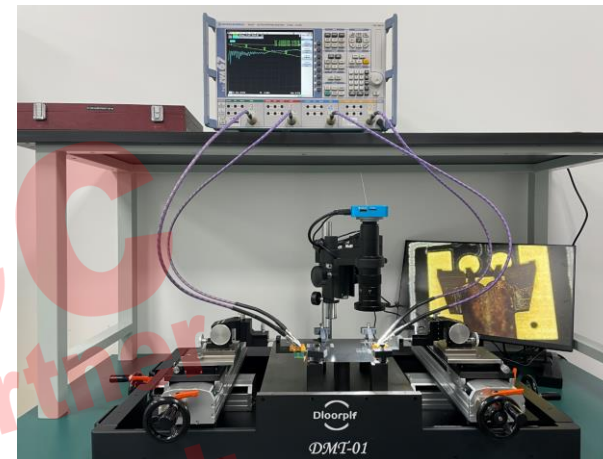
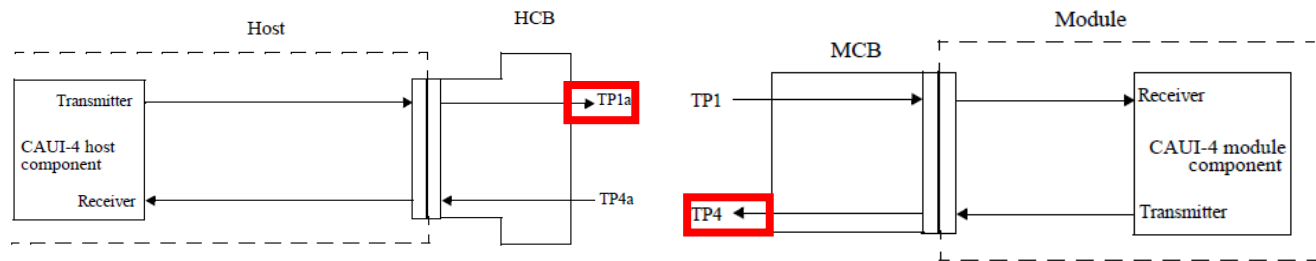


Figure 120C-3—400GAUI-16 chip-to-module insertion loss budget at 13.28 GHz

- 光板
- PCBA



有源SPEC



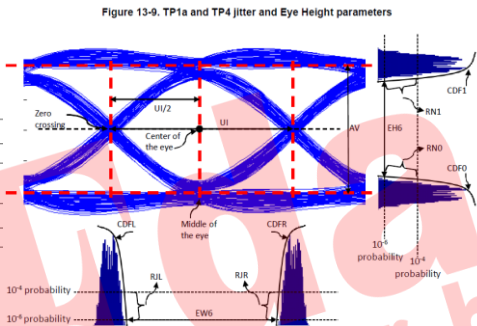
28G-VSR

Table 13-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	900	mV	

Table 13-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	-	900	mV	



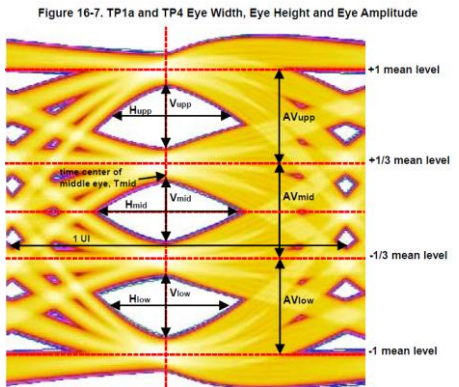
56G-VSR-PAM4

Table 16-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	880	mV	See Note 1

Table 16-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	-	900	mV	



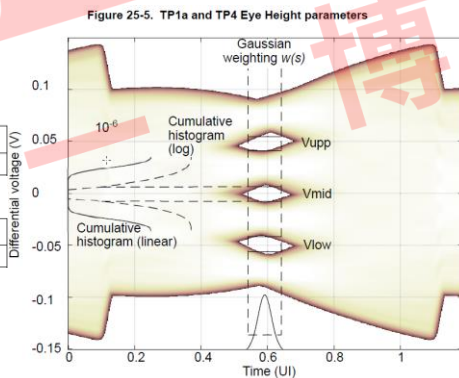
112G-VSR-PAM4

Table 25-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Unit	Conditions
Differential Voltage pk-pk	-	880	mV	See 25.3.4

Table 25-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Unit	Conditions
Differential Voltage, pk-pk	-	880	mV	See 25.3.4



10G SFP+

Eye Mask	X1	Mask hit ratio of 5x10 ⁻⁵ , See D.2 and Figure 19	0.12	UI
Eye Mask	X2		0.33	UI
Eye Mask	Y1		95	mV
Eye Mask	Y2		350	mV

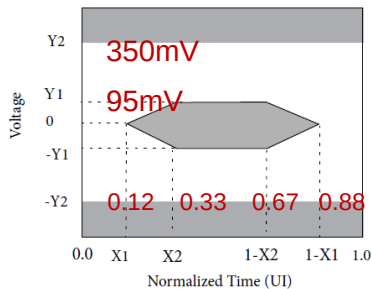
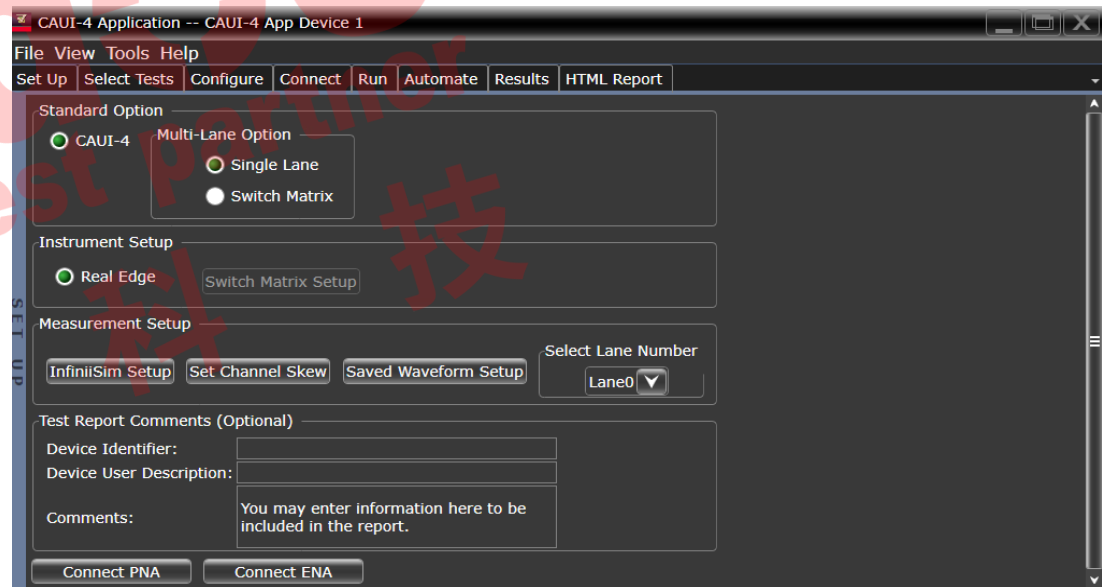
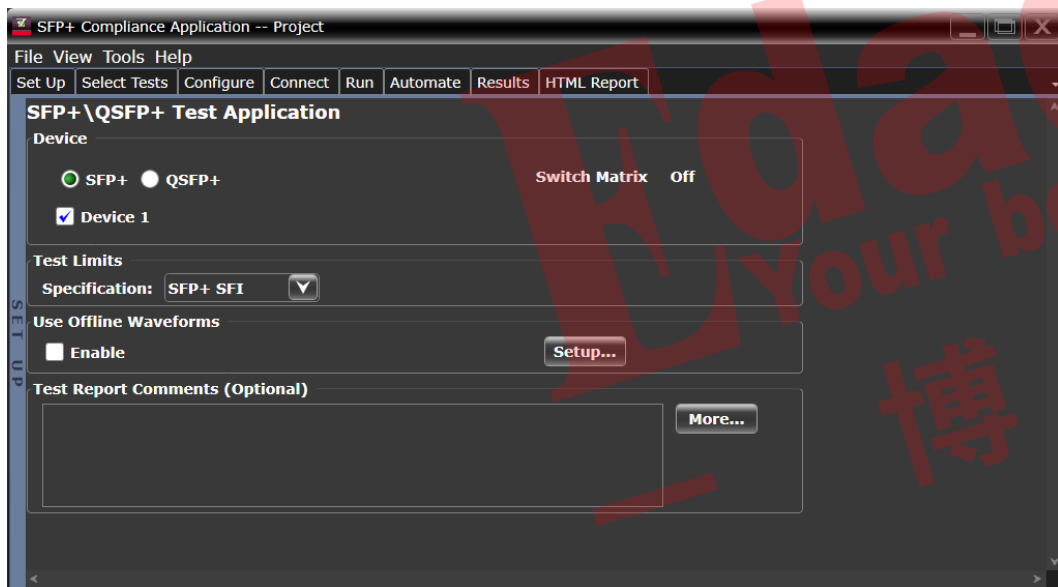
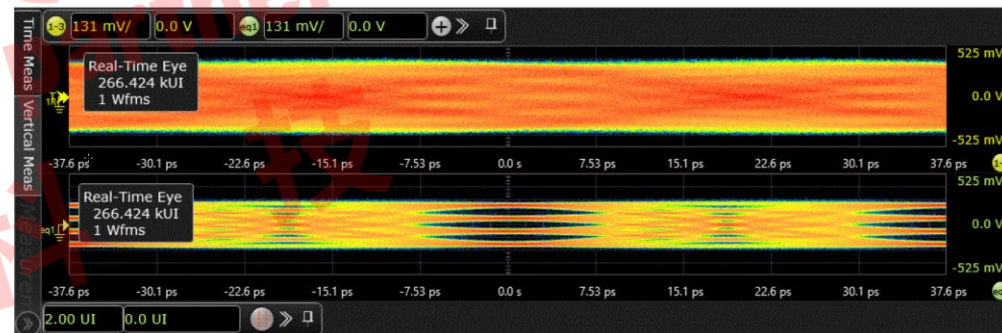


Figure 19 Transmitter Differential Output Compliance Mask at B and B'

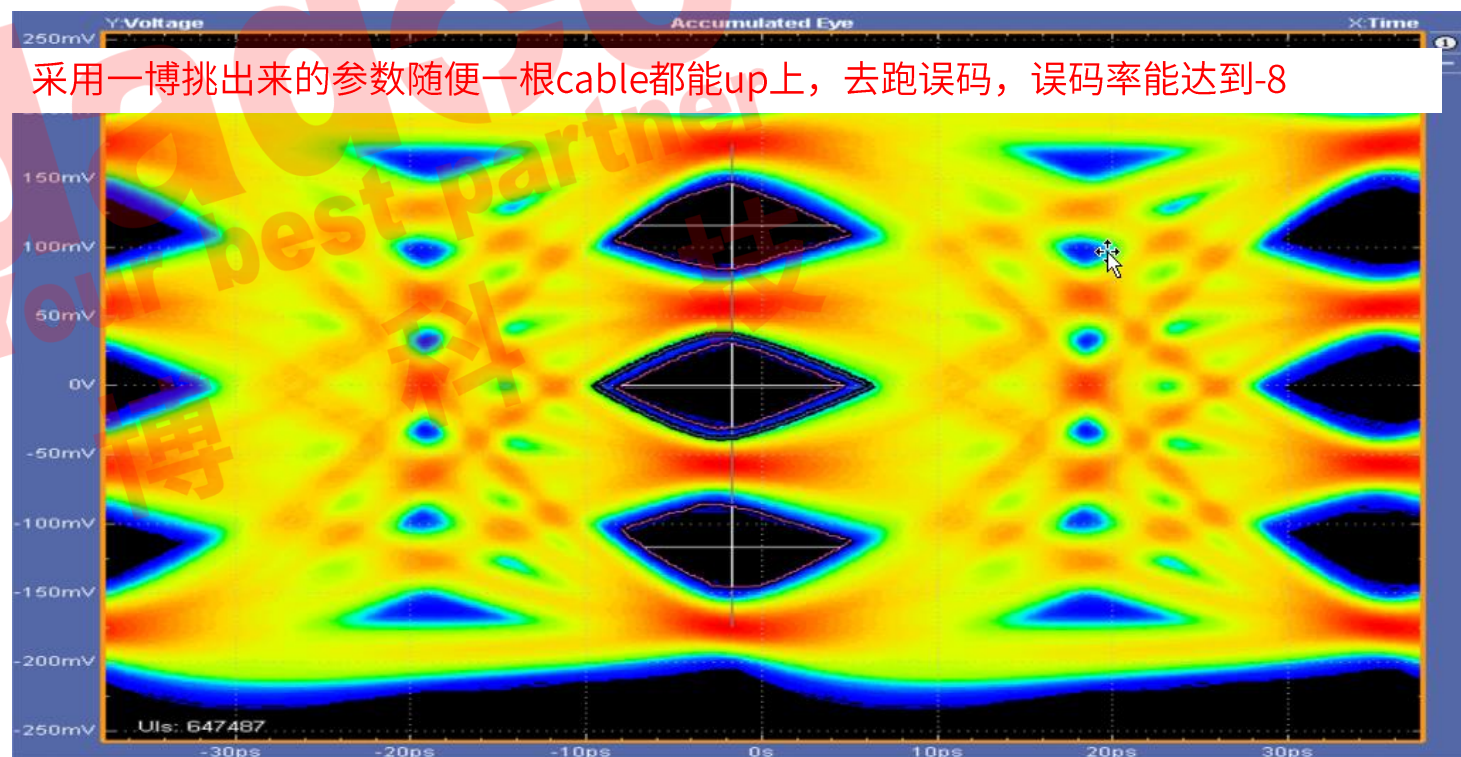
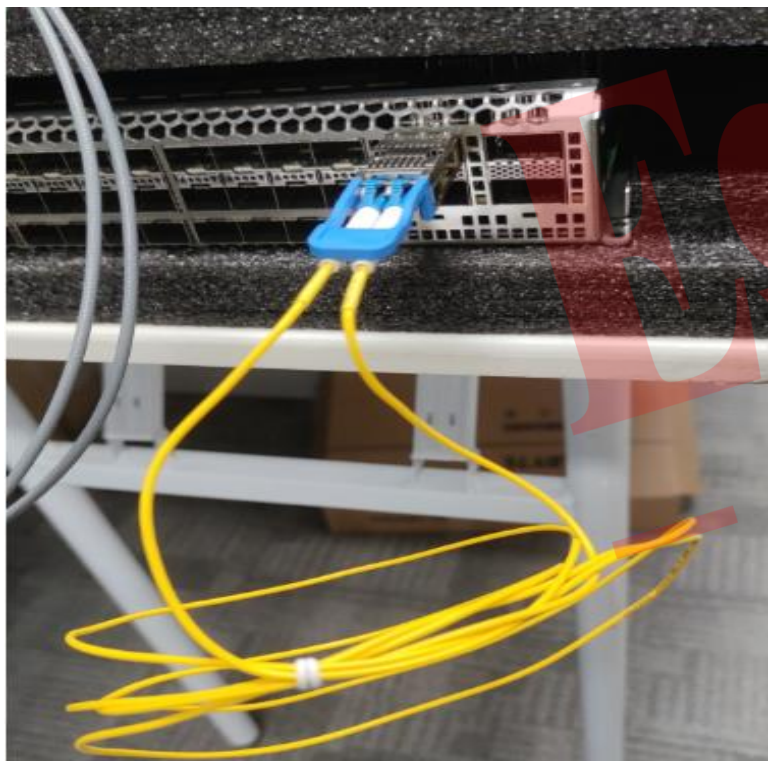
- 10G
- 25G
- 56G
- 112G



- 目前用的比较多的两种接口
- 56G PAM4测试



- 光口信号长度不同、出线层不同，无法用统一的参数
- 环回有误码
- 56G PAM4光口电测试：光环回，用厂家给的参数所有口用任何光纤都link不上，但用在厂家的 Demo板上测试结果很好

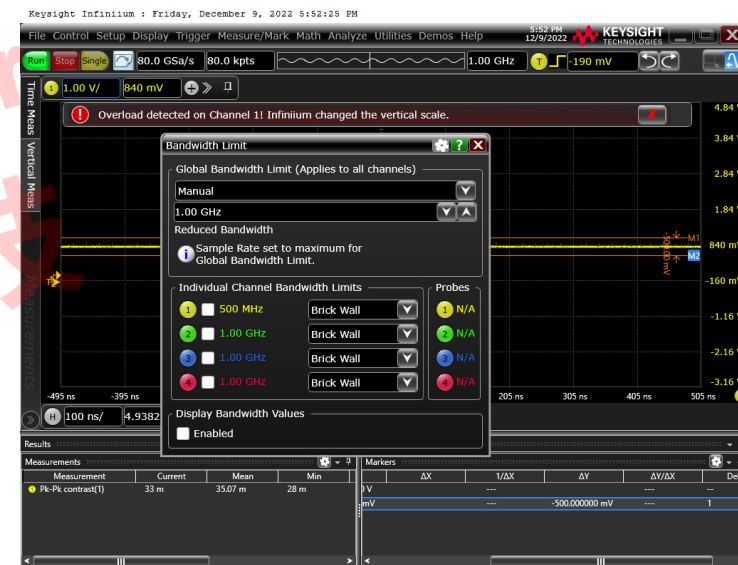
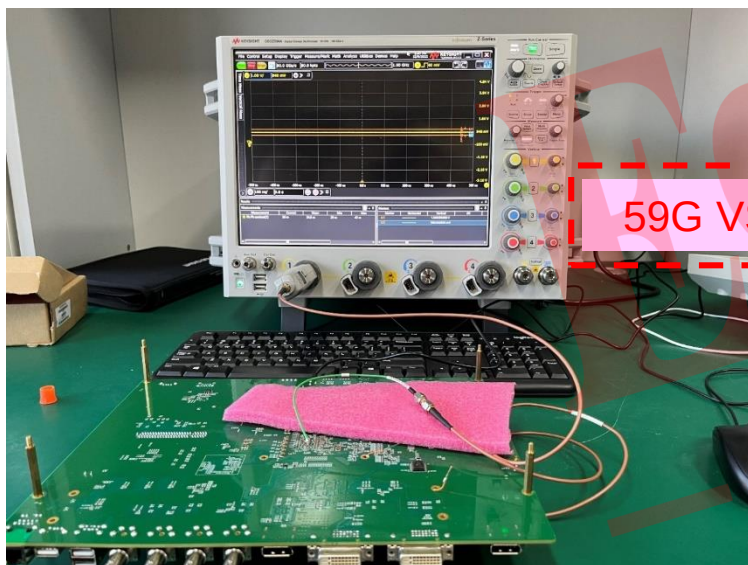


PART 04

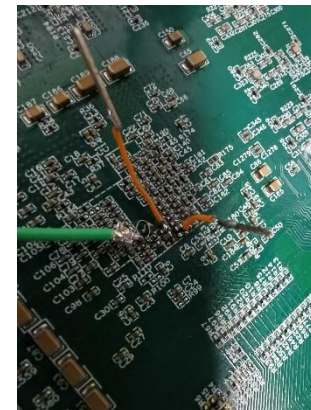
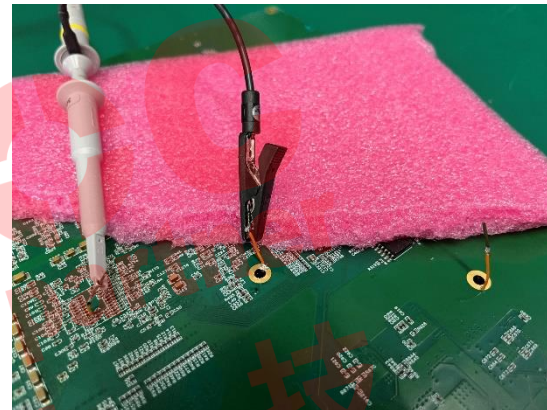
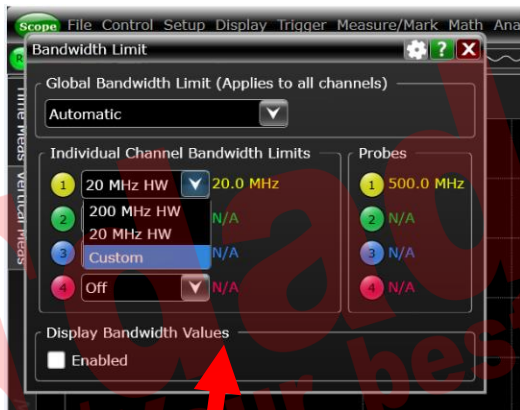
电源测试



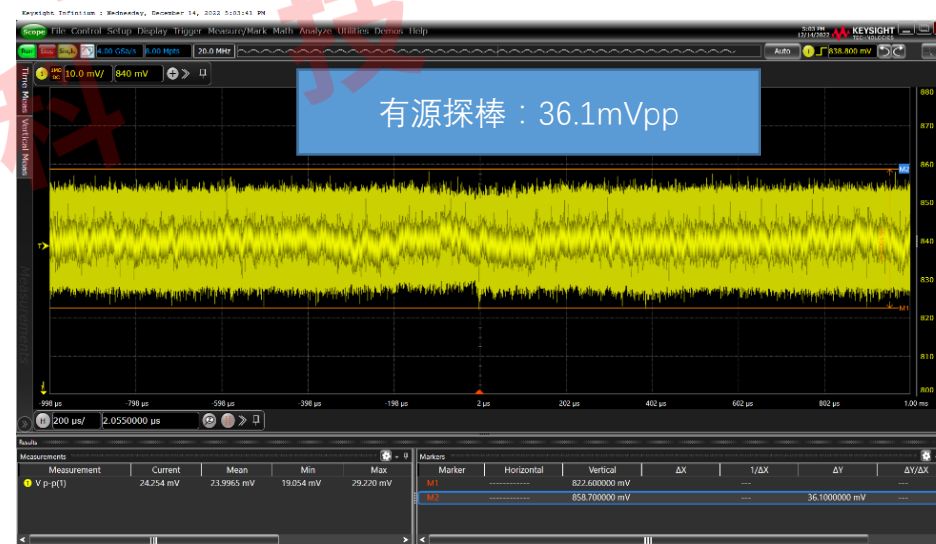
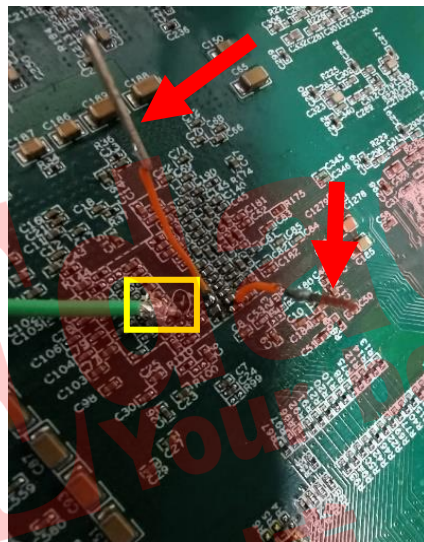
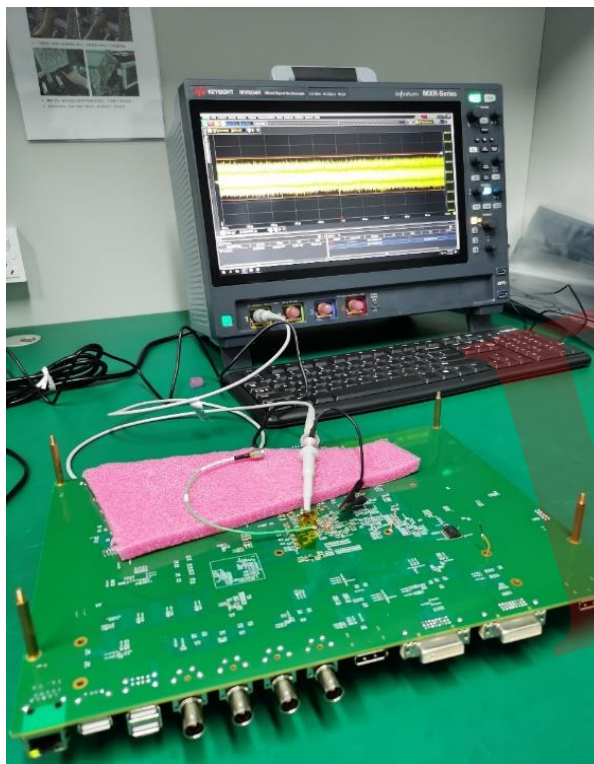
- 示波器：带宽
- 探棒
- 测试手法/设置：人



- 示波器
- 探棒
- 测试手法/设置：人

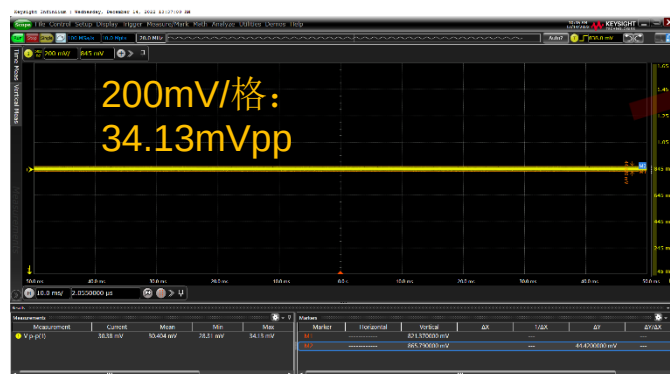
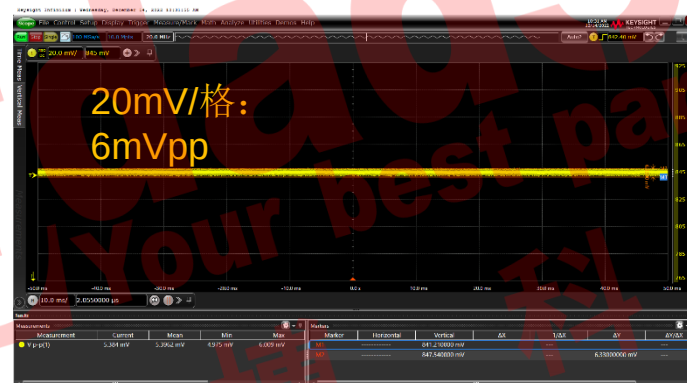
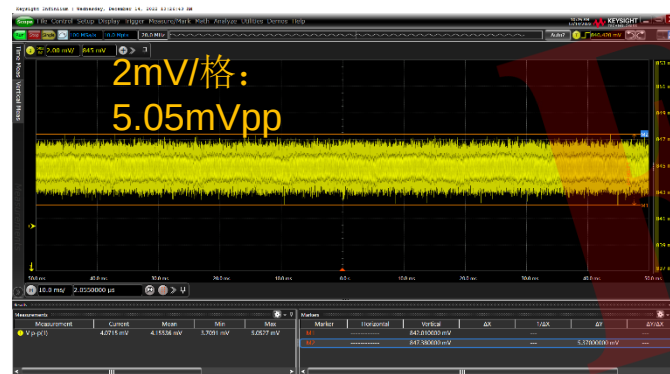
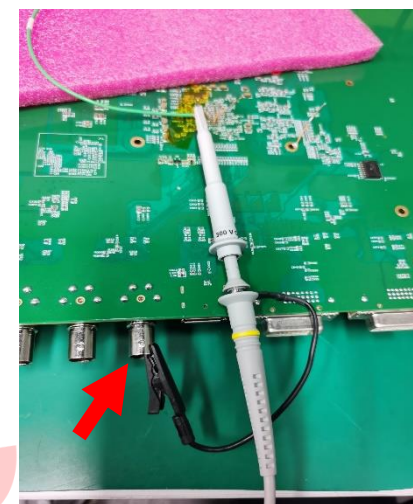
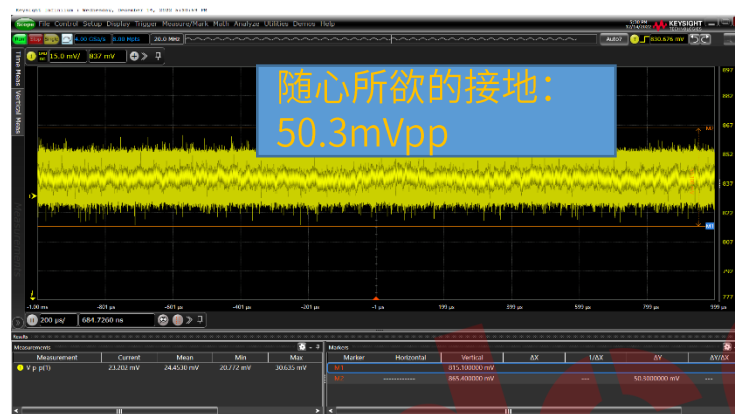


10:1无源探棒 vs.1:1电源探棒



- 示波器
- 探棒
- 测试手法/设置：人

- 刻度
- 接地

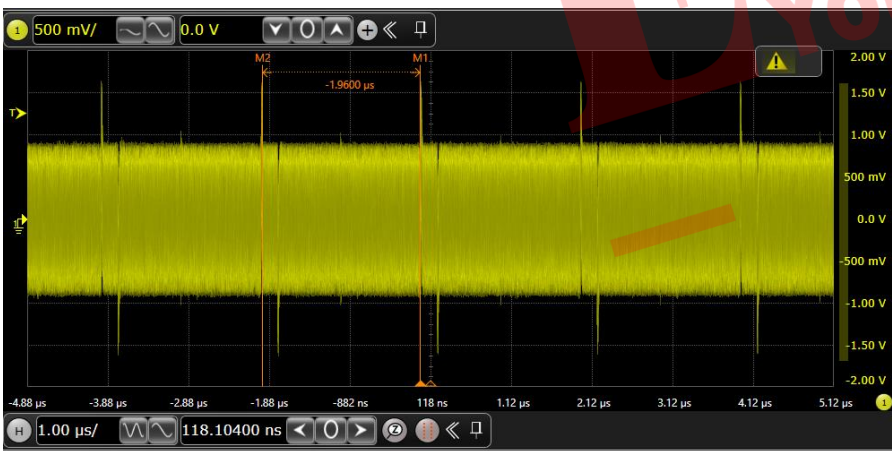


PART 05

总结



- 天时：你越来越重视SI测试
- 地利：我有得心应手的装备
- 人和：我们会测试、能分析



➤ 仪器

- 67G 矢网
- 64G 误码仪
- 59G 示波器
- 33G 示波器
- 6G 示波器
- 2.5G 示波器
- 500M 示波器

➤ 两地实验室

- 深圳
- 珠海

Thank you!

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