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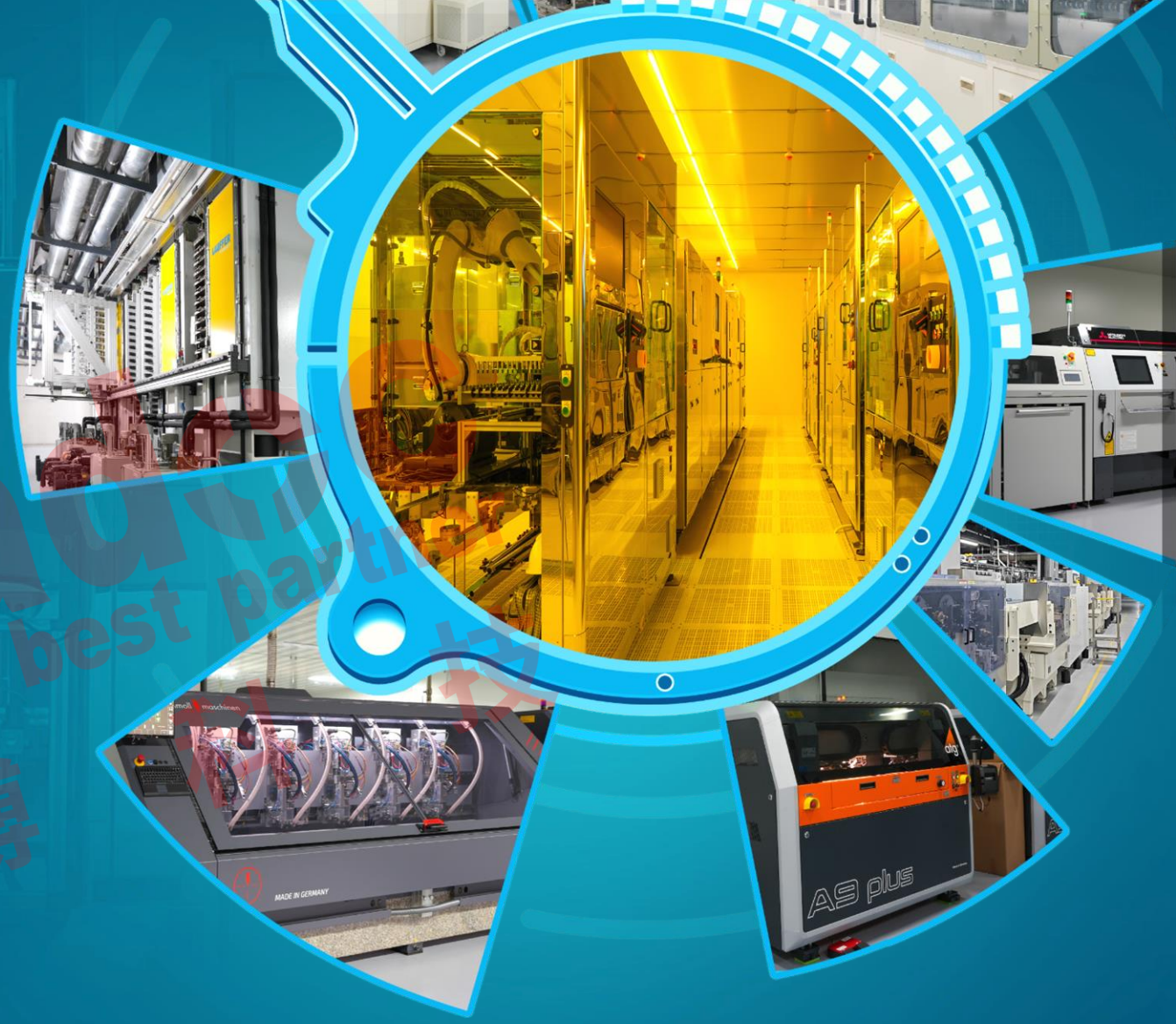
# 深挖阻抗的细节问题

## PCB设计十大误区（外传3）




一博科技-SI研究部

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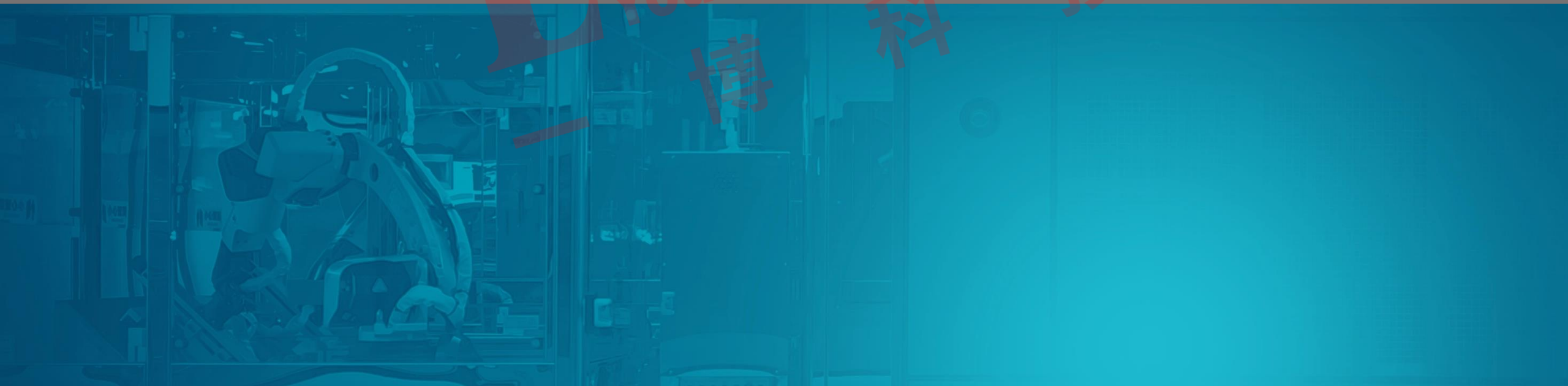
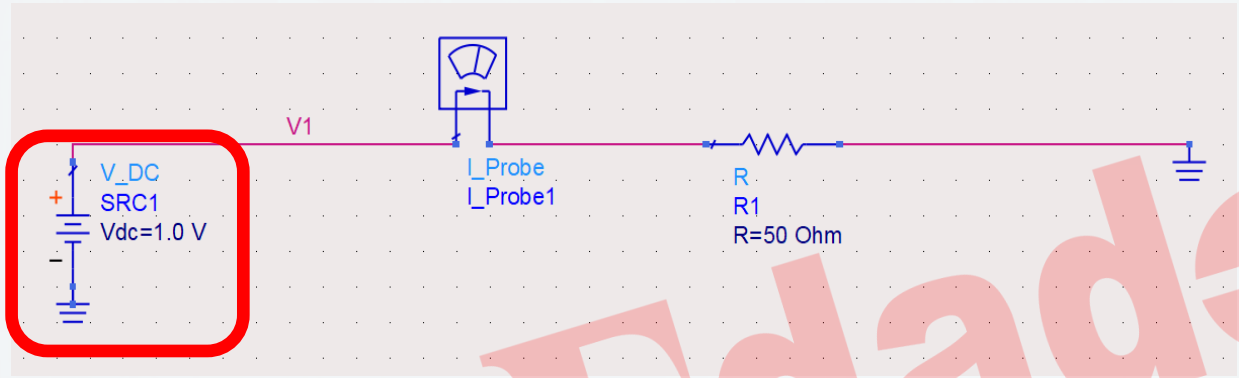
PART 01

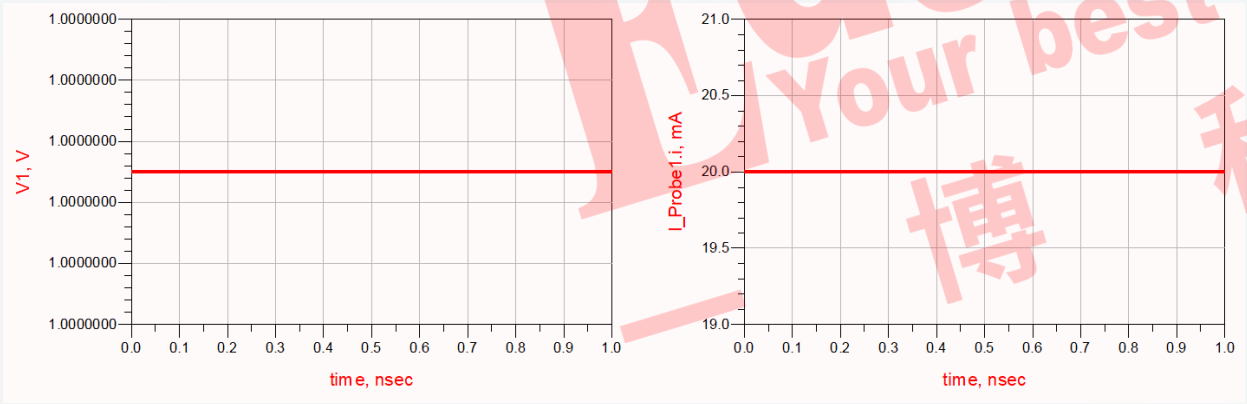
# 阻抗：高速设计的入门

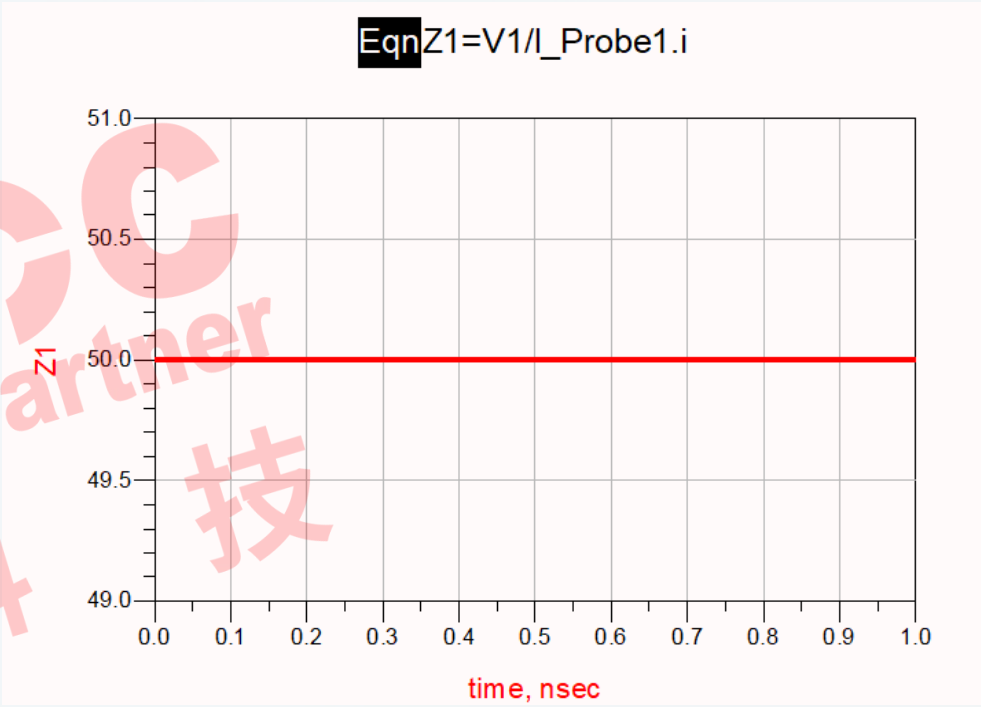


# 电阻与阻抗

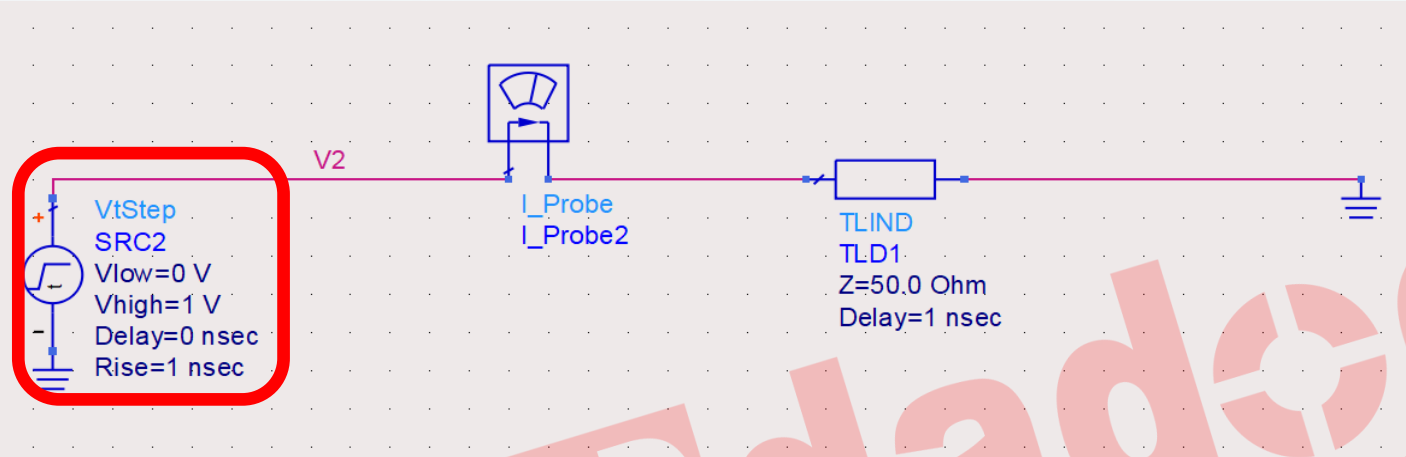
- 到底能不能讲清楚电阻与阻抗的区别?
- 电阻的概念大家估计很好理解

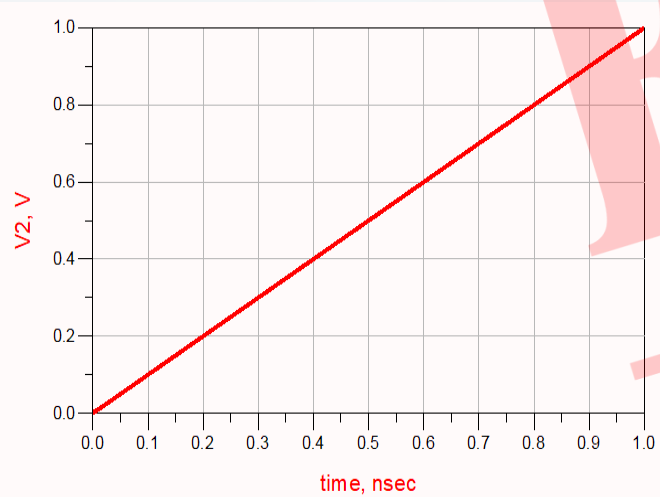


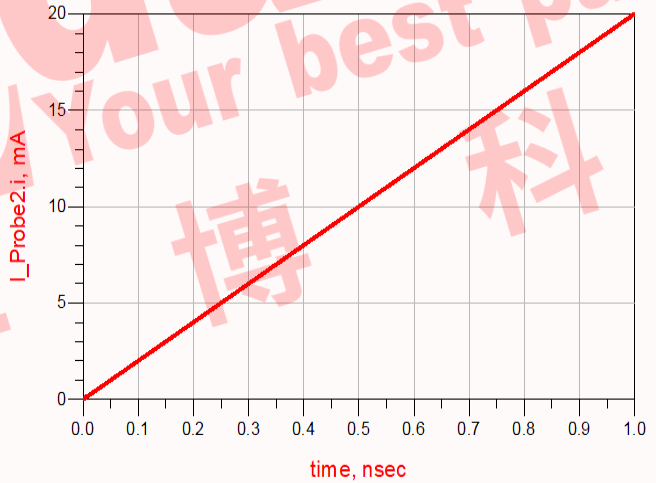



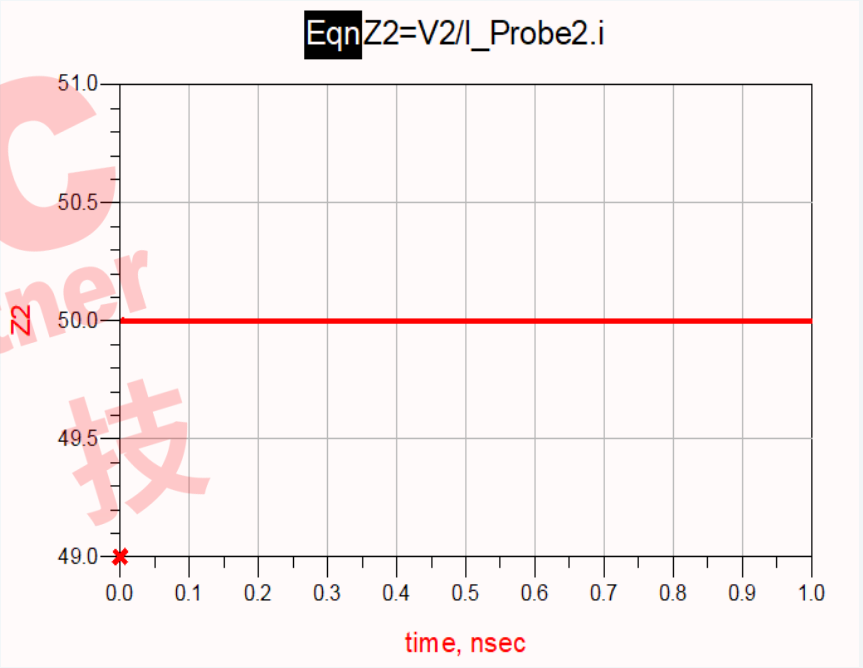



- 那阻抗是怎么表征的呢?

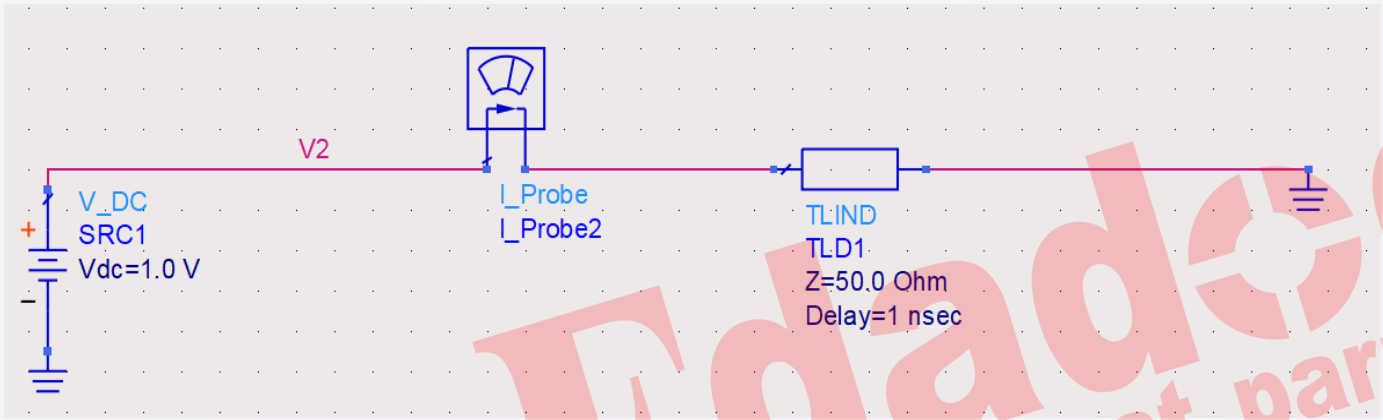


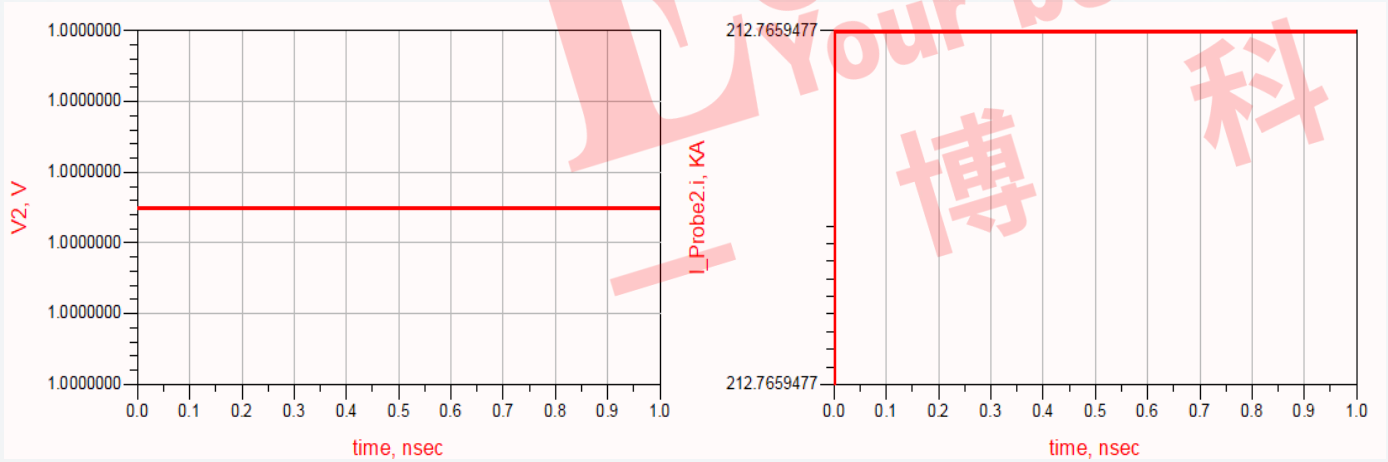



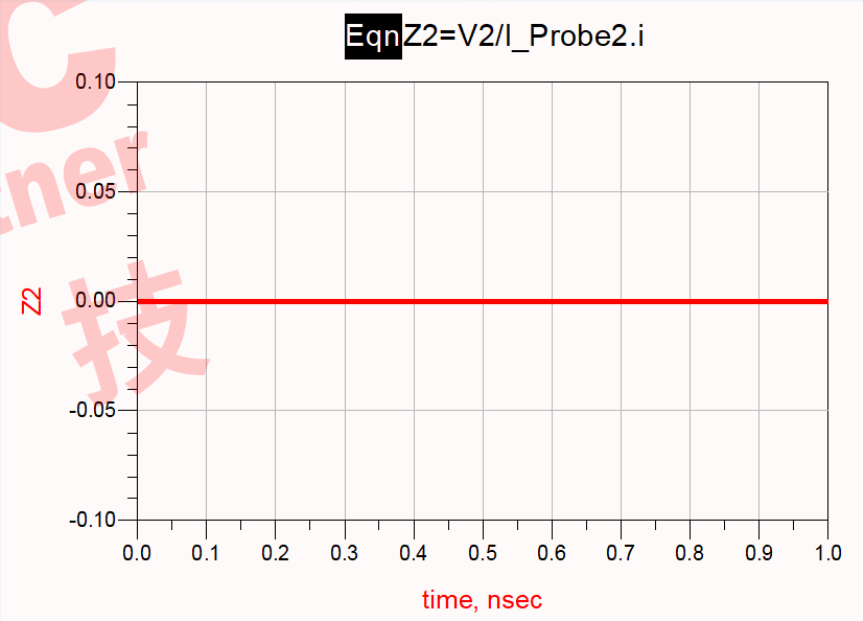



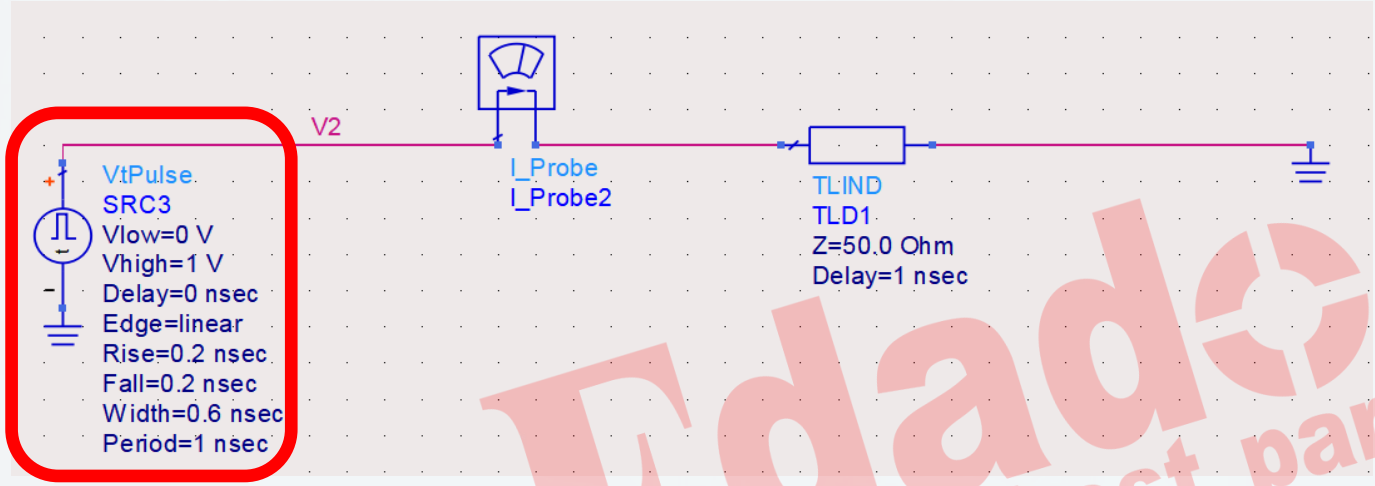
- 什么叫变化的电压或电流才能产生阻抗
- 这样会有阻抗吗?

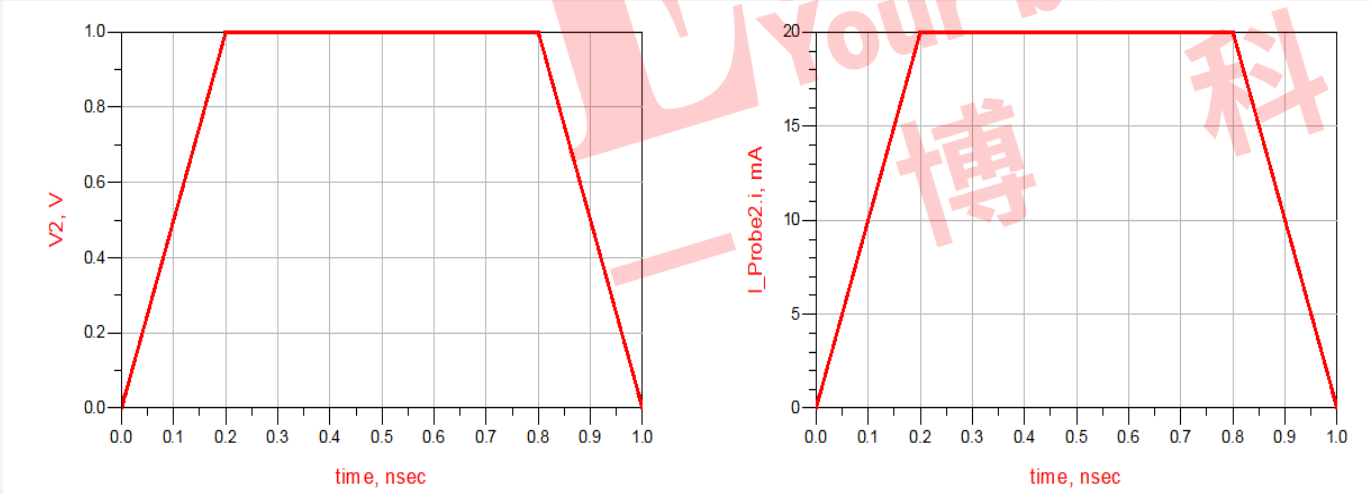


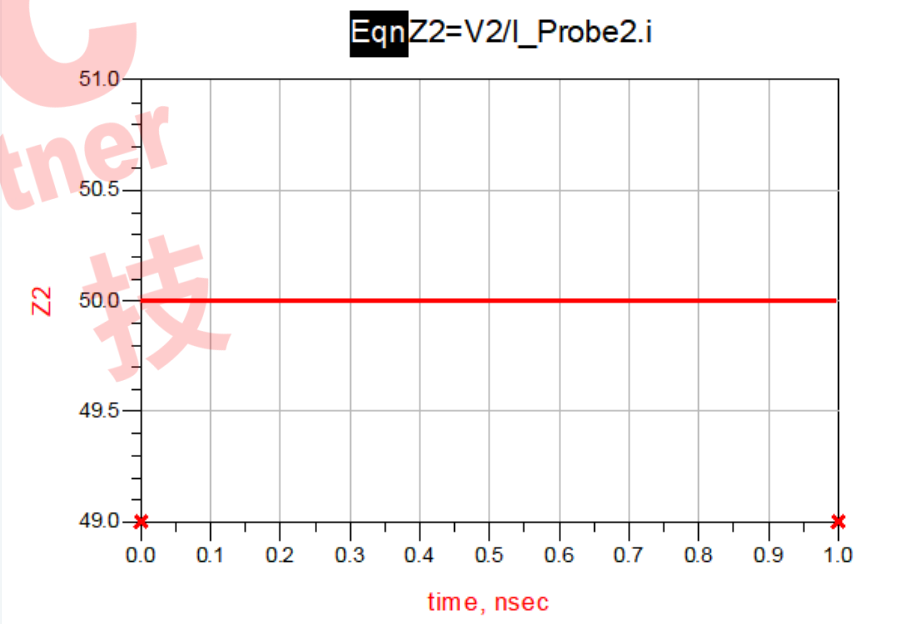



- 一定只能是阶跃信号才能表征出阻抗吗?
- 脉冲信号可以吗?

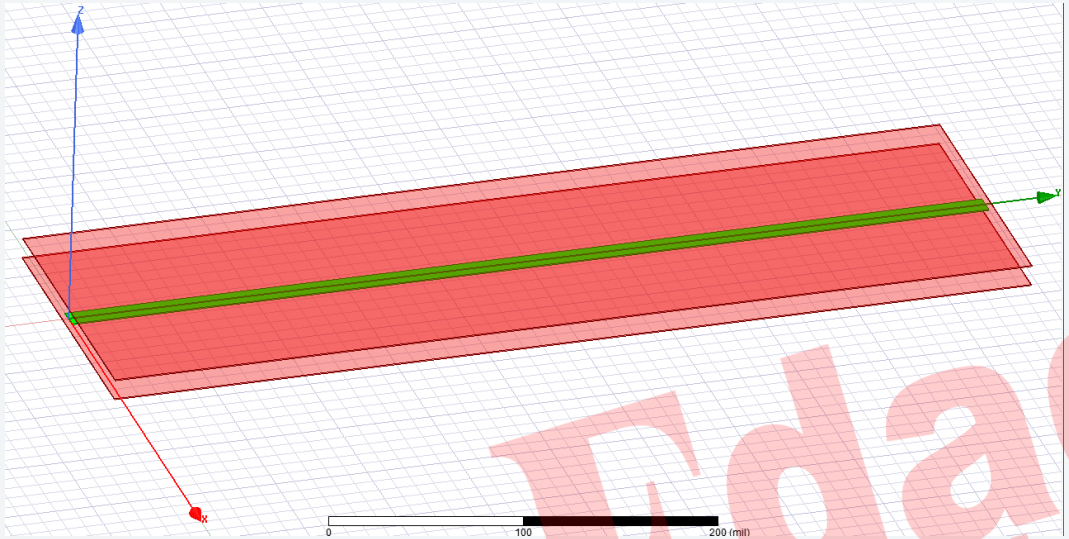


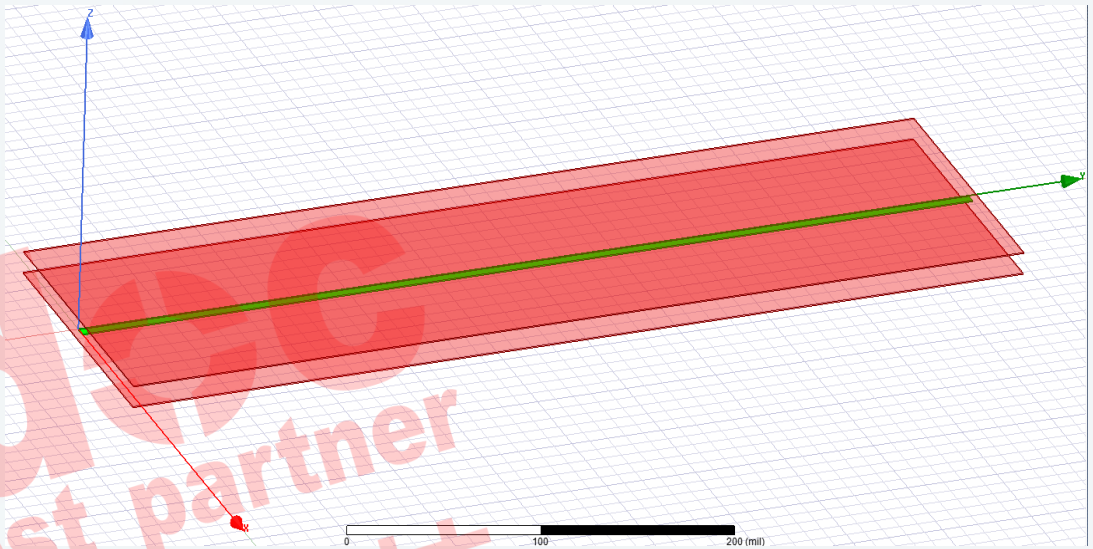



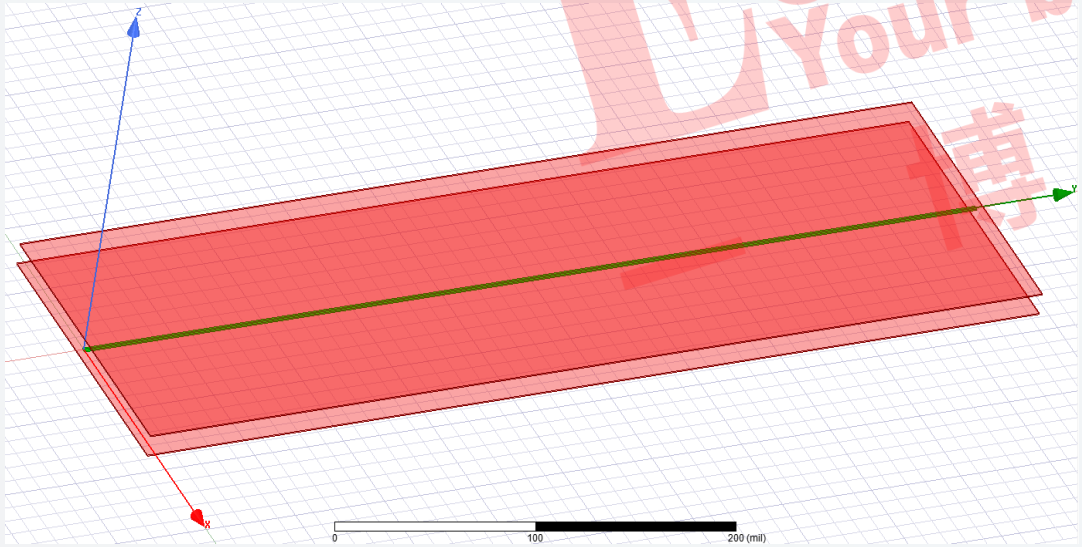



# 场的方式来看阻抗

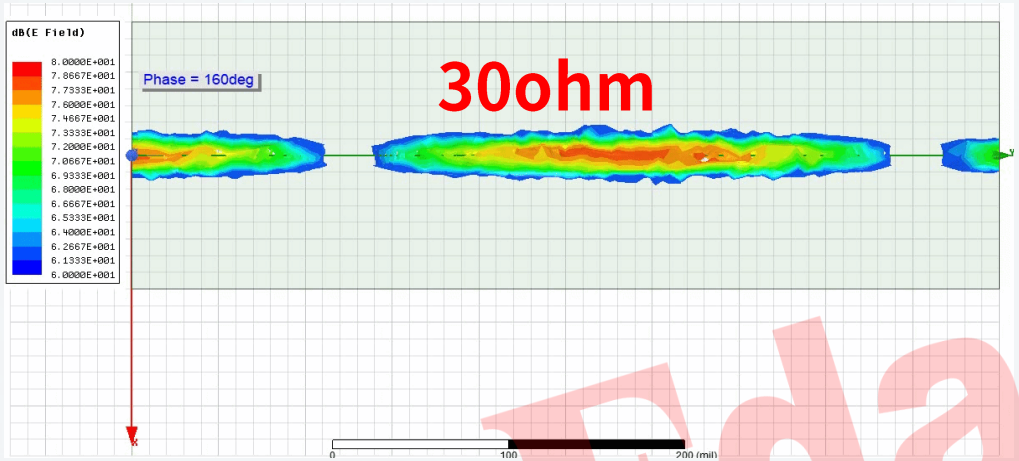
- 30ohm，50ohm，70ohm的3D传输性模型

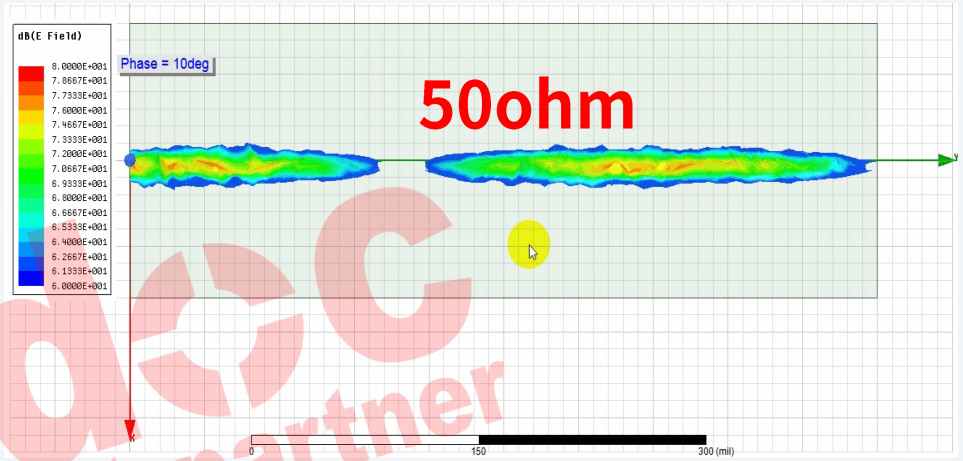


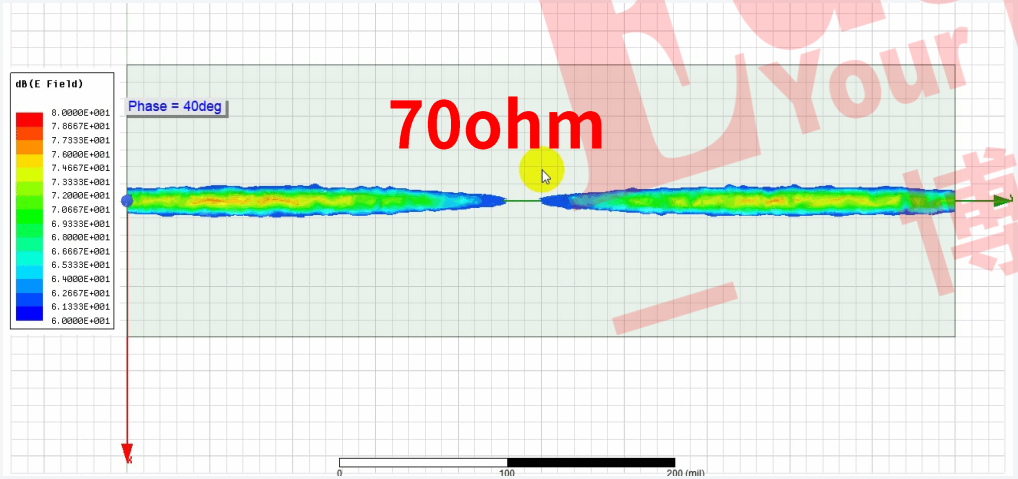



- 阻抗就是阻碍电磁场传输的能力，阻抗不同，阻碍电磁场的程度不同



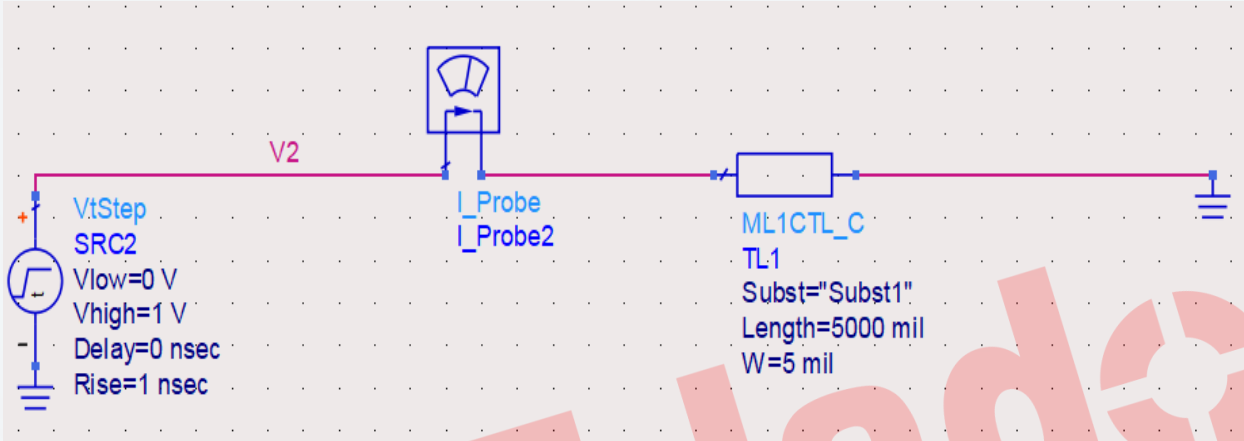



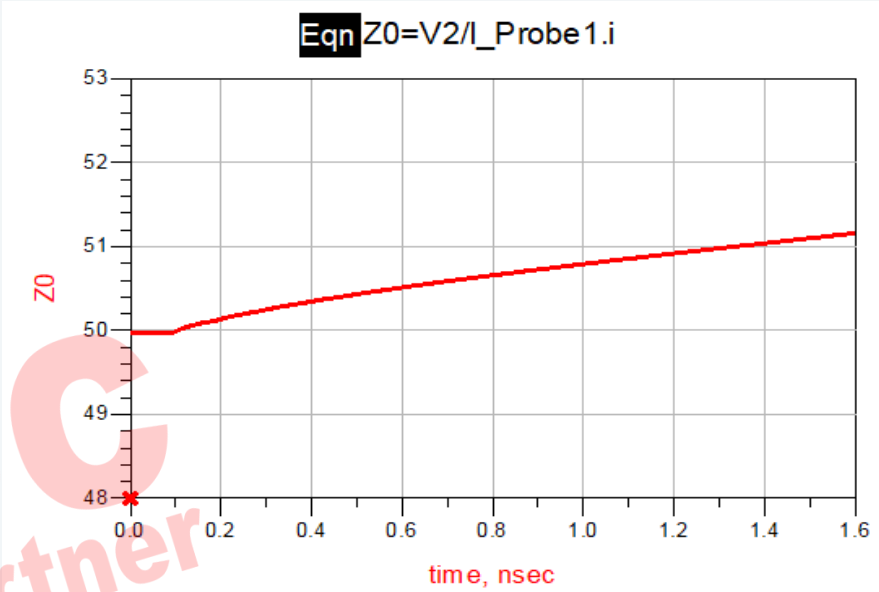



# 电阻和阻抗并存

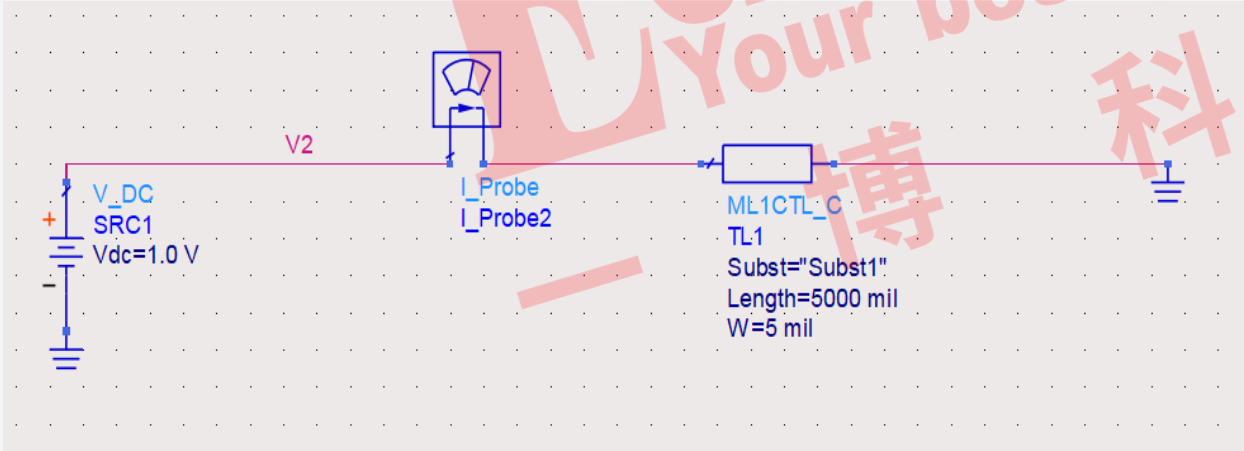
- 真实的传输线既有电阻又有阻抗……

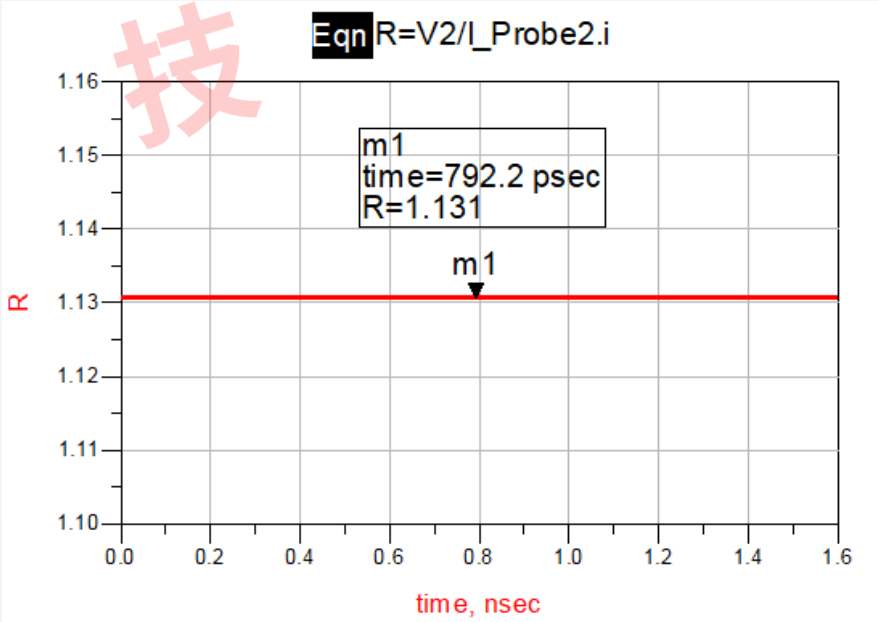
**阻抗**



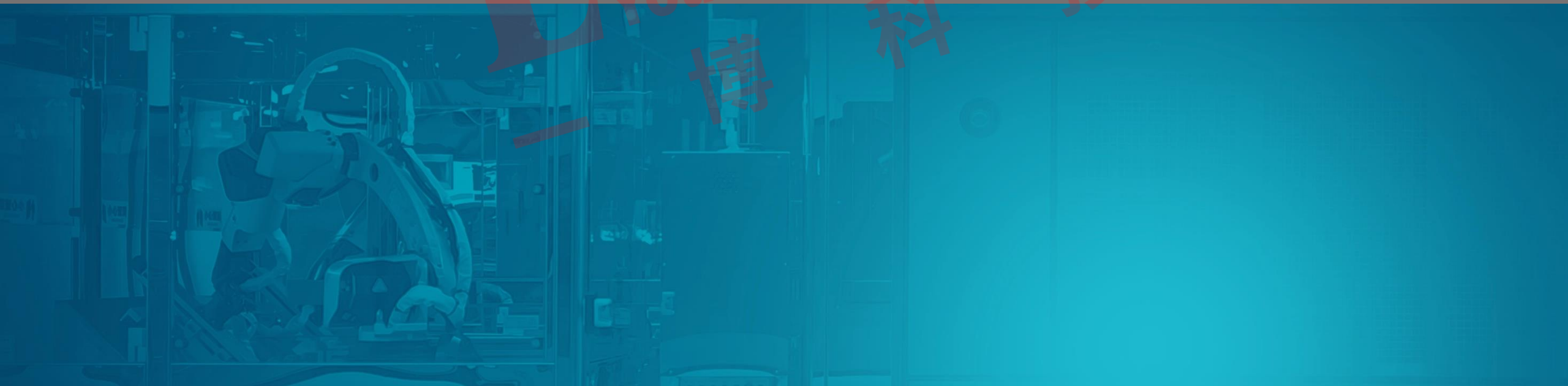

**电阻**



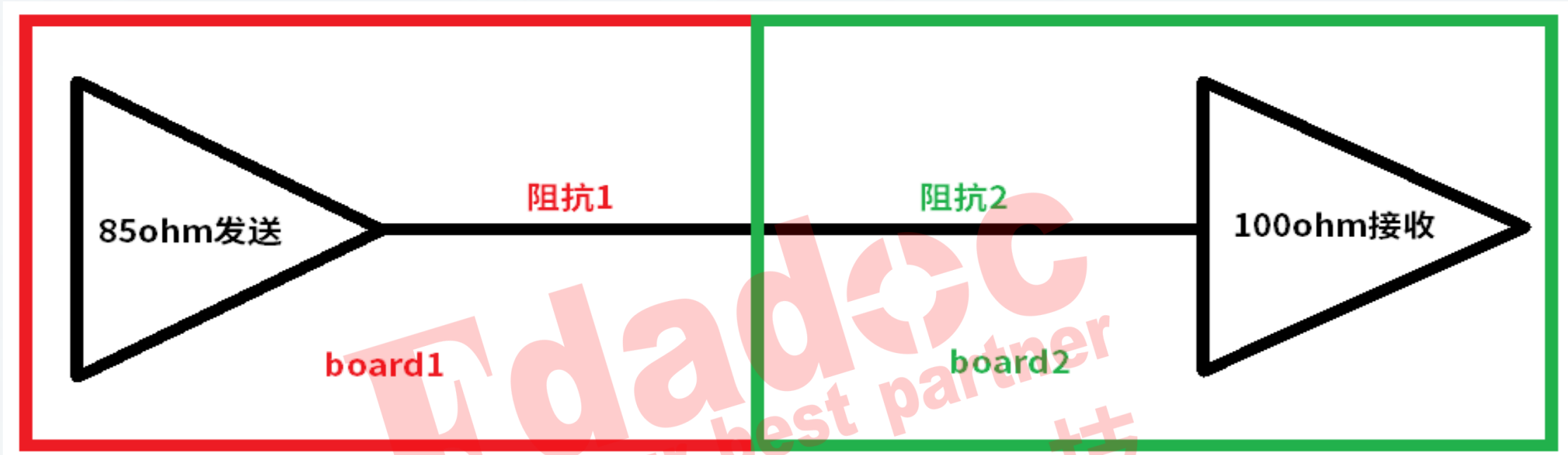
PART 02

# 设计上选对阻抗值其实更重要



# 两端芯片内阻不一样

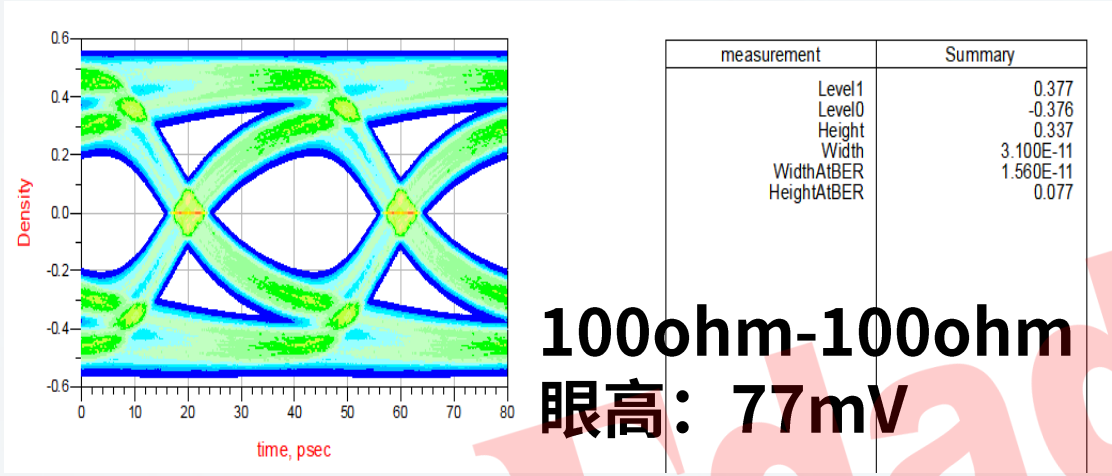
- 两块板的阻抗要怎么控?




- case1：board1-100ohm，board2-100ohm；
- case2：board1-85ohm，board2-85ohm；
- case3：board1-85ohm，board2-100ohm；
- case4：board1-92.5ohm，board2-92.5ohm；

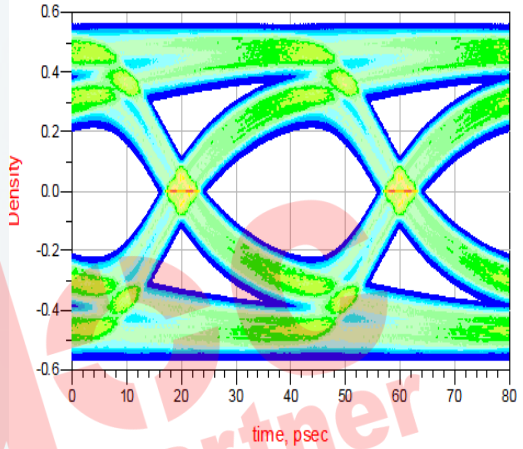
# 两端芯片内阻不一样

- 两块板的传输线阻抗控制不同



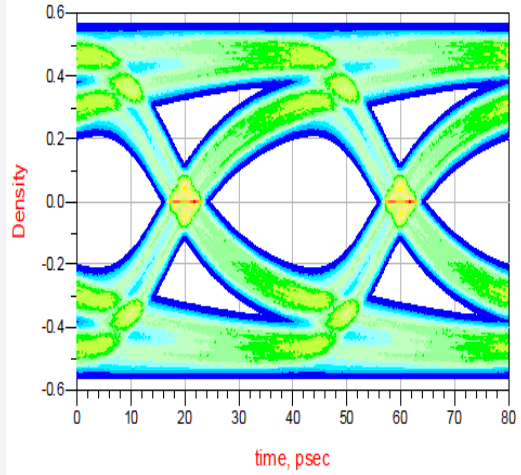

| measurement | Summary |
|---|---|
| Level1 | 0.377 |
| Level0 | -0.376 |
| Height | 0.337 |
| Width | 3.100E-11 |
| WidthAtBER | 1.560E-11 |
| HeightAtBER | 0.077 |

**100ohm-100ohm**
**眼高：77mV**



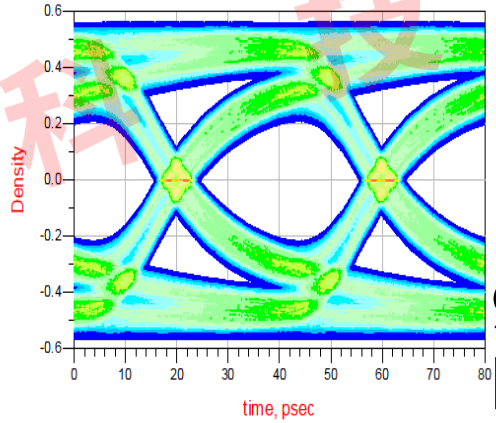

| measurement | Summary |
|---|---|
| Level1 | 0.386 |
| Level0 | -0.385 |
| Height | 0.367 |
| Width | 3.160E-11 |
| WidthAtBER | 1.840E-11 |
| HeightAtBER | 0.135 |

**85ohm-85ohm**
**眼高：135mV**




| measurement | Summary |
|---|---|
| Level1 | 0.383 |
| Level0 | -0.382 |
| Height | 0.350 |
| Width | 3.160E-11 |
| WidthAtBER | 1.700E-11 |
| HeightAtBER | 0.102 |

**85ohm-100ohm**
**眼高：102mV**

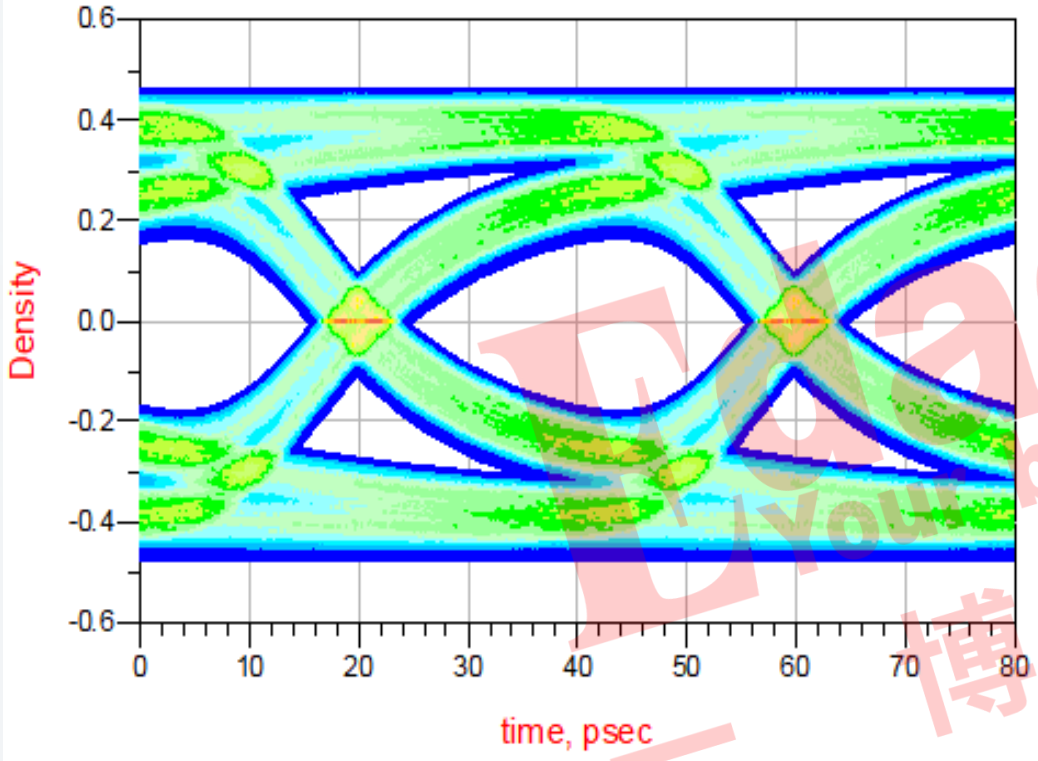



| measurement | Summary |
|---|---|
| Level1 | 0.382 |
| Level0 | -0.382 |
| Height | 0.355 |
| Width | 3.140E-11 |
| WidthAtBER | 1.740E-11 |
| HeightAtBER | 0.109 |

**92.5ohm-92.5ohm**
**眼高：109mV**

两端芯片内阻不一样

- 如果搞反了，case5：board1-100ohm，board2-85ohm；

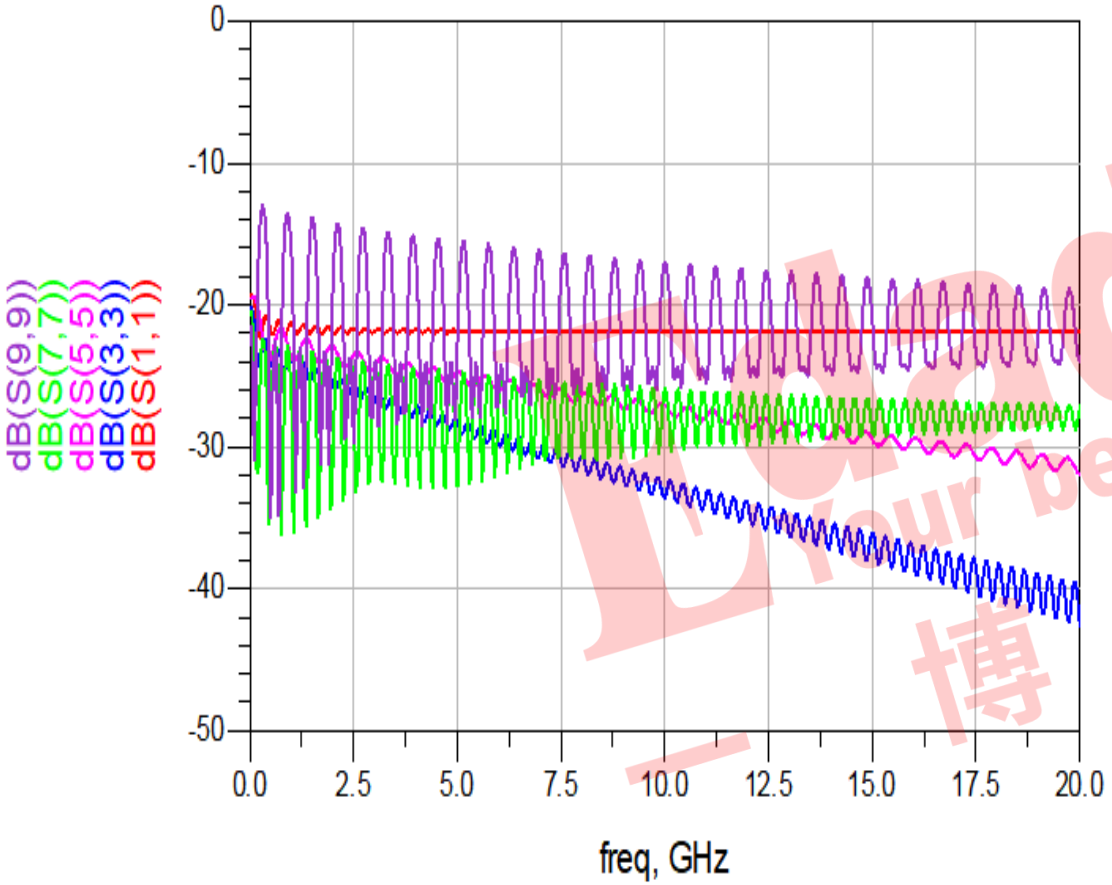


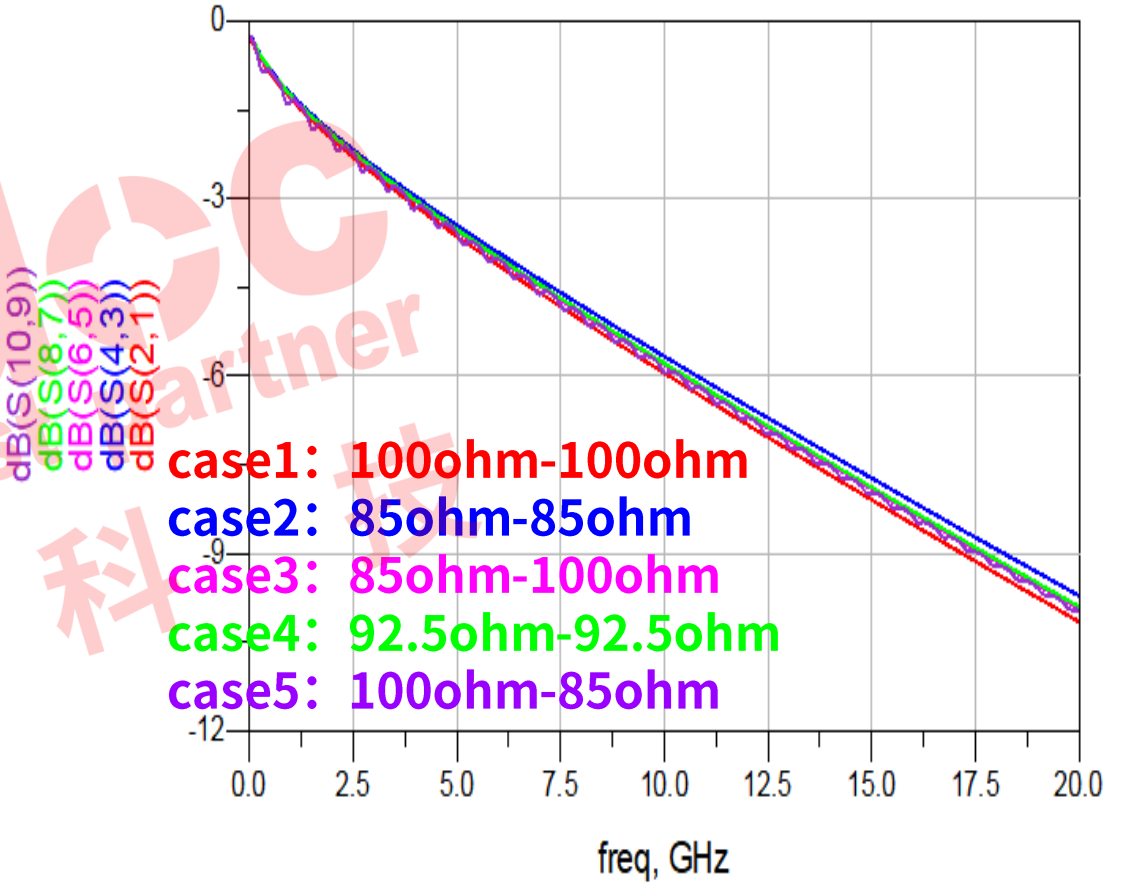

| measurement | Summary |
|---|---|
| Level1 | 0.317 |
| Level0 | -0.317 |
| Height | 0.283 |
| Width | 3.100E-11 |
| WidthAtBER | 1.640E-11 |
| HeightAtBER | 0.080 |

**100ohm-85ohm**
**眼高：80mV**

# 两端芯片内阻不一样

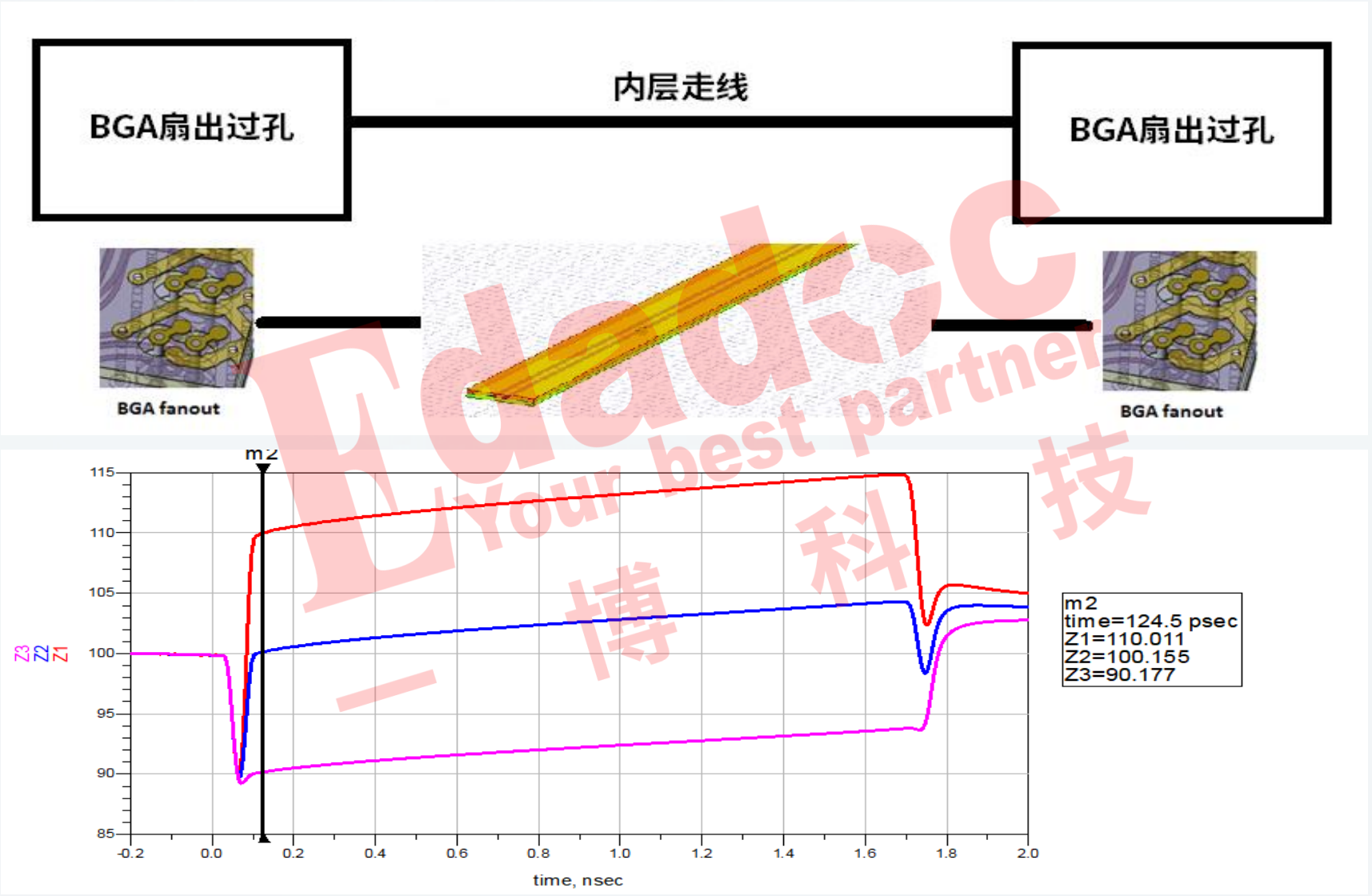
- 从插损回损上找原因



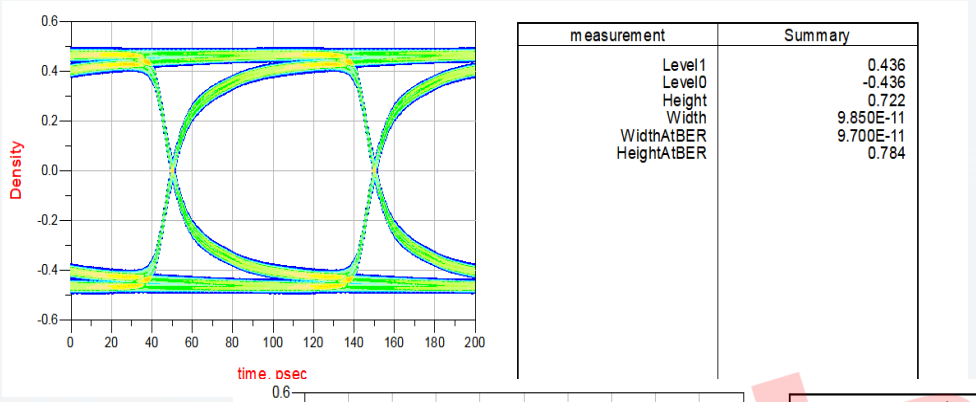
# 100欧姆真的是最好吗？

- 两端的过孔只能优化到90欧姆的情况下，传输线的阻抗控100是最好的吗？



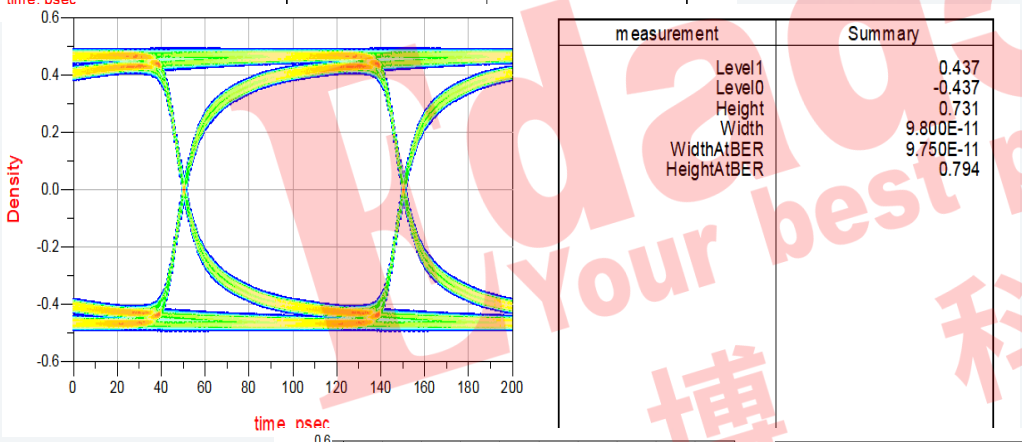
# 100欧姆真的是最好吗？

- 10G信号的眼图结果



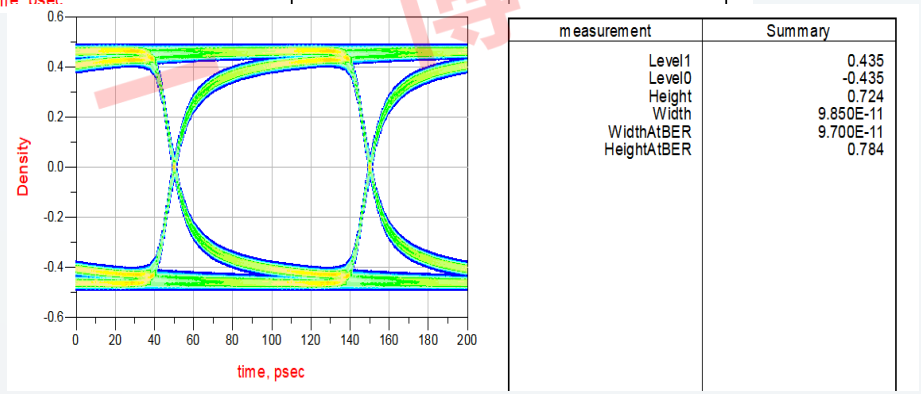

| measurement | Summary |
|---|---|
| Level1 | 0.436 |
| Level0 | -0.436 |
| Height | 0.722 |
| Width | 9.850E-11 |
| WidthAtBER | 9.700E-11 |
| HeightAtBER | 0.784 |

**110欧姆：眼高784mV**




| measurement | Summary |
|---|---|
| Level1 | 0.437 |
| Level0 | -0.437 |
| Height | 0.731 |
| Width | 9.800E-11 |
| WidthAtBER | 9.750E-11 |
| HeightAtBER | 0.794 |

**100欧姆：眼高794mV**

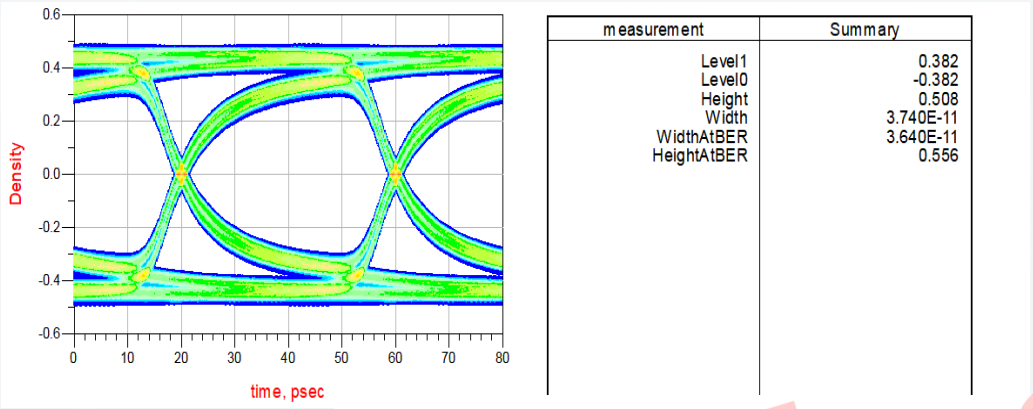



| measurement | Summary |
|---|---|
| Level1 | 0.435 |
| Level0 | -0.435 |
| Height | 0.724 |
| Width | 9.850E-11 |
| WidthAtBER | 9.700E-11 |
| HeightAtBER | 0.784 |

**90欧姆：眼高784mV**

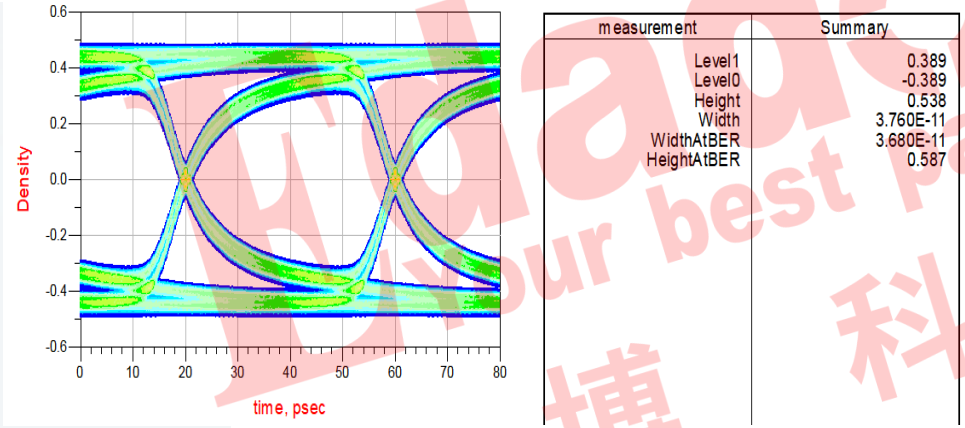
# 100欧姆真的是最好吗？

- 25G信号的眼图结果



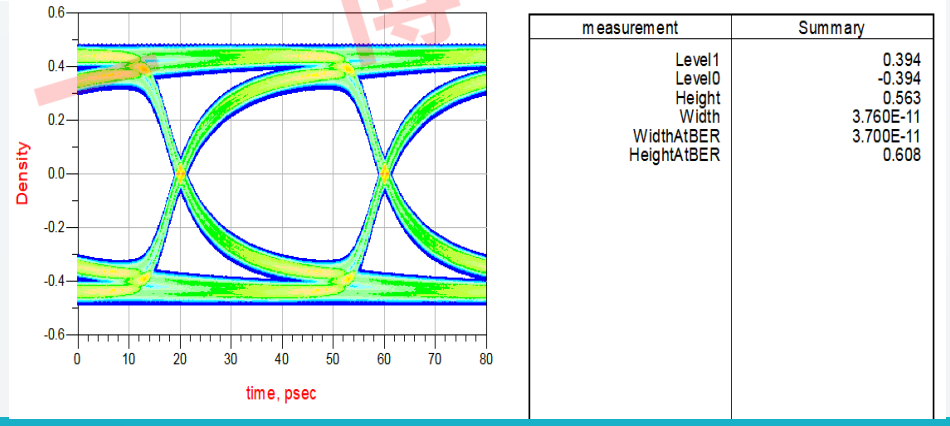

| measurement | Summary |
|---|---|
| Level1 | 0.382 |
| Level0 | -0.382 |
| Height | 0.508 |
| Width | 3.740E-11 |
| WidthAtBER | 3.640E-11 |
| HeightAtBER | 0.556 |

**110欧姆：眼高556mV**




| measurement | Summary |
|---|---|
| Level1 | 0.389 |
| Level0 | -0.389 |
| Height | 0.538 |
| Width | 3.760E-11 |
| WidthAtBER | 3.680E-11 |
| HeightAtBER | 0.587 |

**100欧姆：眼高587mV**

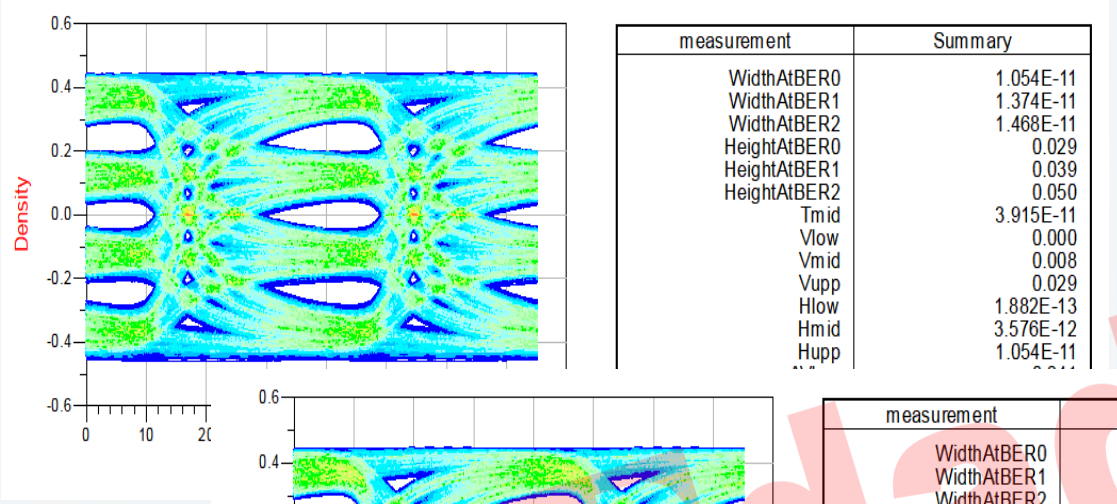



| measurement | Summary |
|---|---|
| Level1 | 0.394 |
| Level0 | -0.394 |
| Height | 0.563 |
| Width | 3.760E-11 |
| WidthAtBER | 3.700E-11 |
| HeightAtBER | 0.608 |

**90欧姆：眼高608mV**

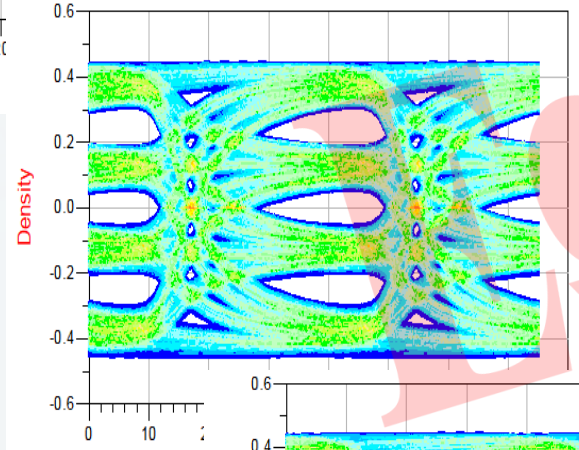
# 100欧姆真的是最好吗？

- 56G-PAM4信号的眼图结果



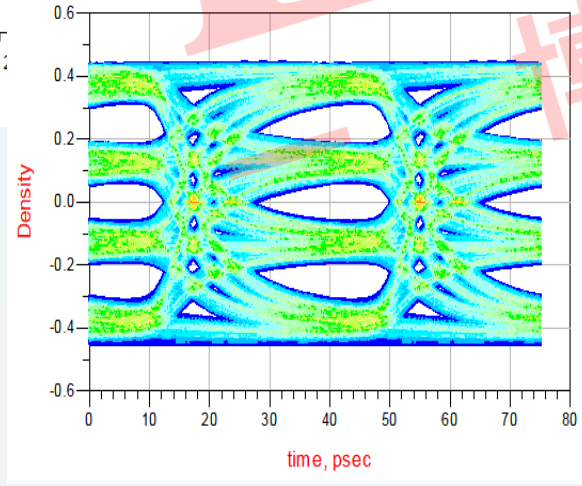

| measurement | Summary |
|---|---|
| WidthAtBER0 | 1.054E-11 |
| WidthAtBER1 | 1.374E-11 |
| WidthAtBER2 | 1.468E-11 |
| HeightAtBER0 | 0.029 |
| HeightAtBER1 | 0.039 |
| HeightAtBER2 | 0.050 |
| Tmid | 3.915E-11 |
| Vlow | 0.000 |
| Vmid | 0.008 |
| Vupp | 0.029 |
| Hlow | 1.882E-13 |
| Hmid | 3.576E-12 |
| Hupp | 1.054E-11 |

**110欧姆：眼高29mV**




| measurement | Summary |
|---|---|
| WidthAtBER0 | 1.468E-11 |
| WidthAtBER1 | 1.638E-11 |
| WidthAtBER2 | 1.769E-11 |
| HeightAtBER0 | 0.050 |
| HeightAtBER1 | 0.058 |
| HeightAtBER2 | 0.075 |
| Tmid | 3.878E-11 |
| Vlow | 0.022 |
| Vmid | 0.025 |
| Vupp | 0.056 |
| Hlow | 1.016E-11 |
| Hmid | 1.280E-11 |
| Hupp | 1.449E-11 |

**100欧姆：眼高50mV**

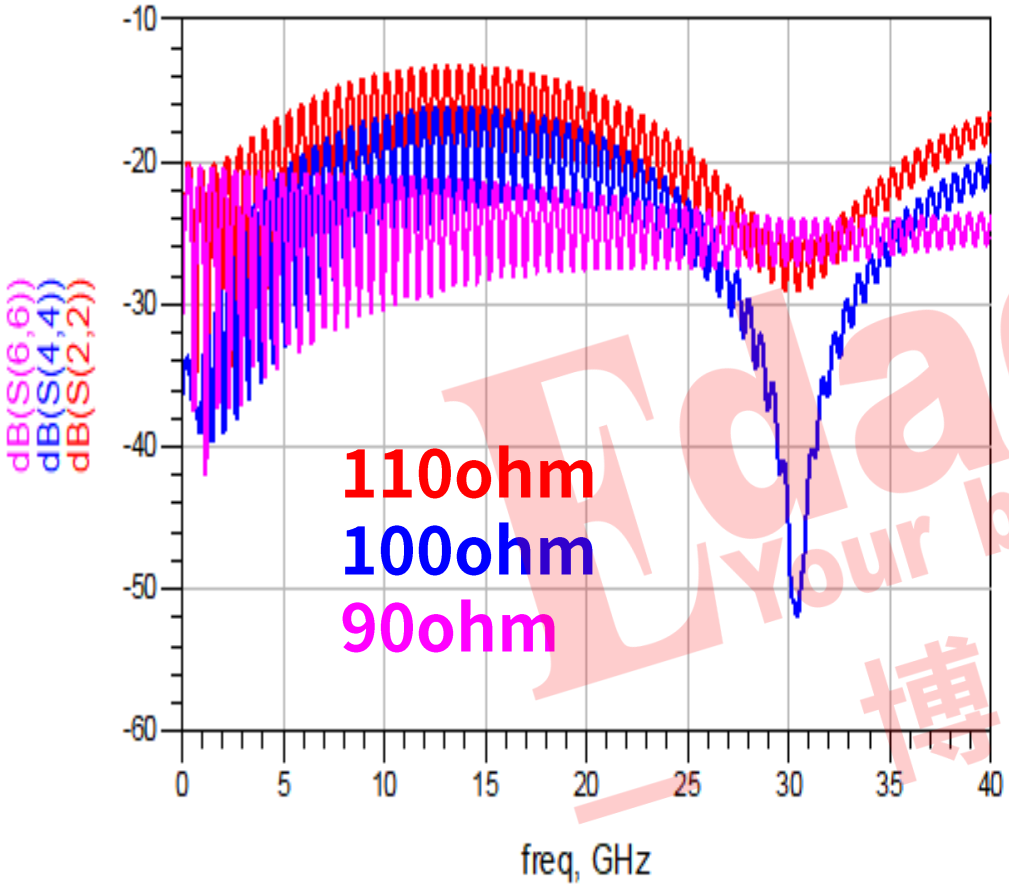


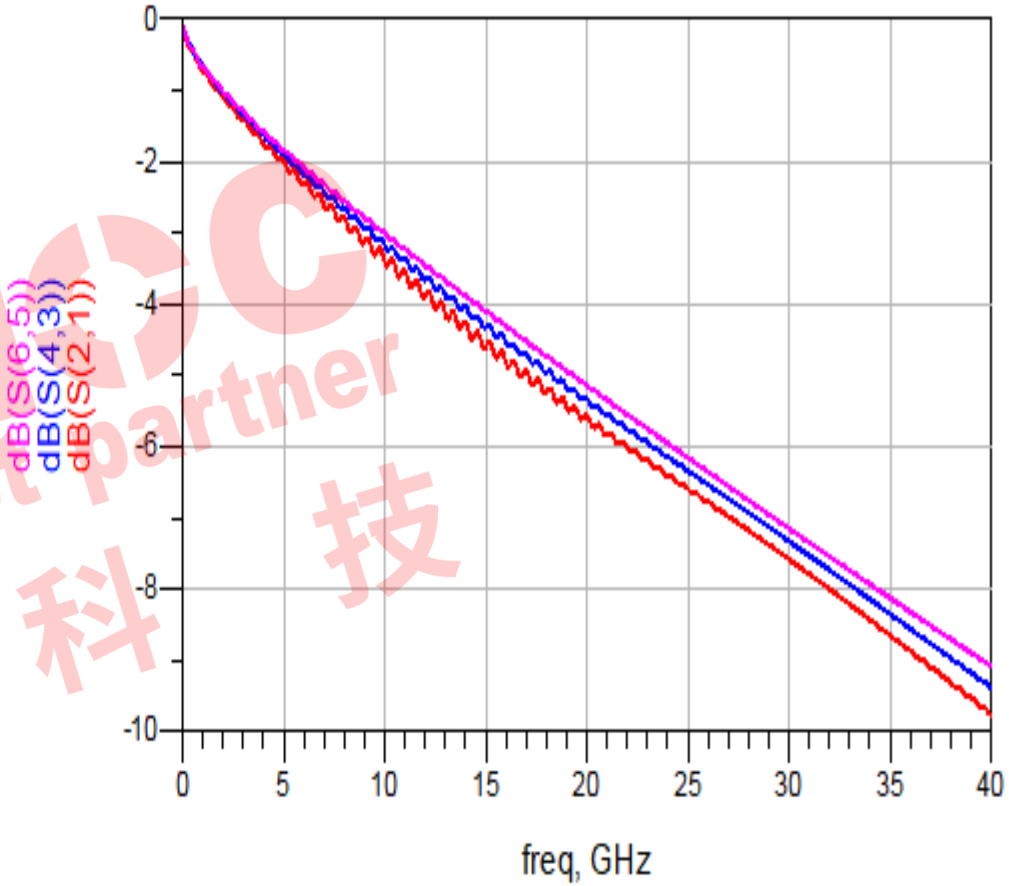

| measurement | Summary |
|---|---|
| WidthAtBER0 | 1.769E-11 |
| WidthAtBER1 | 1.845E-11 |
| WidthAtBER2 | 1.920E-11 |
| HeightAtBER0 | 0.073 |
| HeightAtBER1 | 0.071 |
| HeightAtBER2 | 0.099 |
| Tmid | 3.878E-11 |
| Vlow | 0.042 |
| Vmid | 0.035 |
| Vupp | 0.068 |
| Hlow | 1.336E-11 |
| Hmid | 1.525E-11 |
| Hupp | 1.619E-11 |
| AVlow | 0.248 |
| AVmid | 0.249 |
| AVupp | 0.248 |

**90欧姆：眼高71mV**

# 100欧姆真的是最好吗？

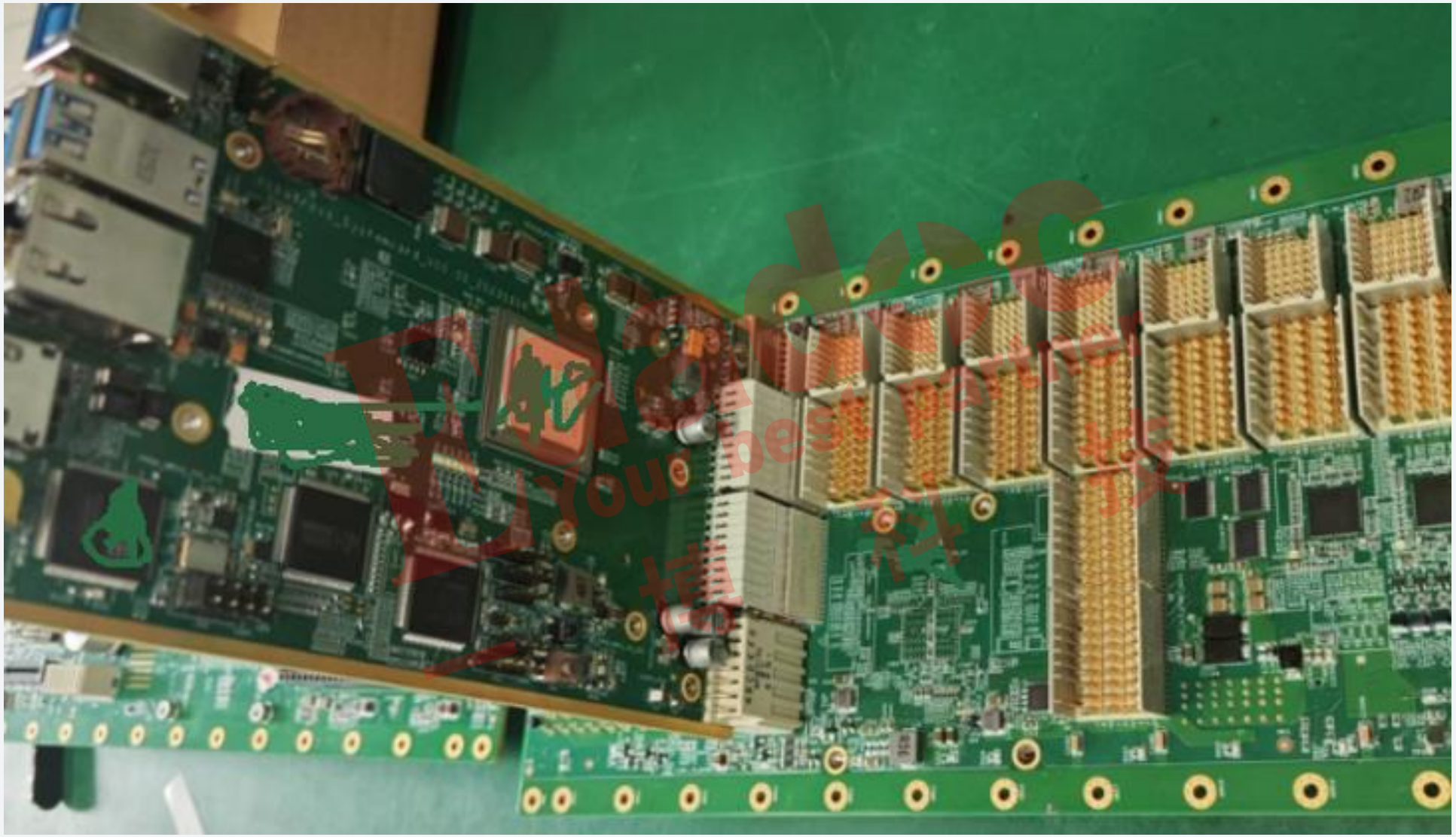
- 从插损回损来看就能知道原因。。。



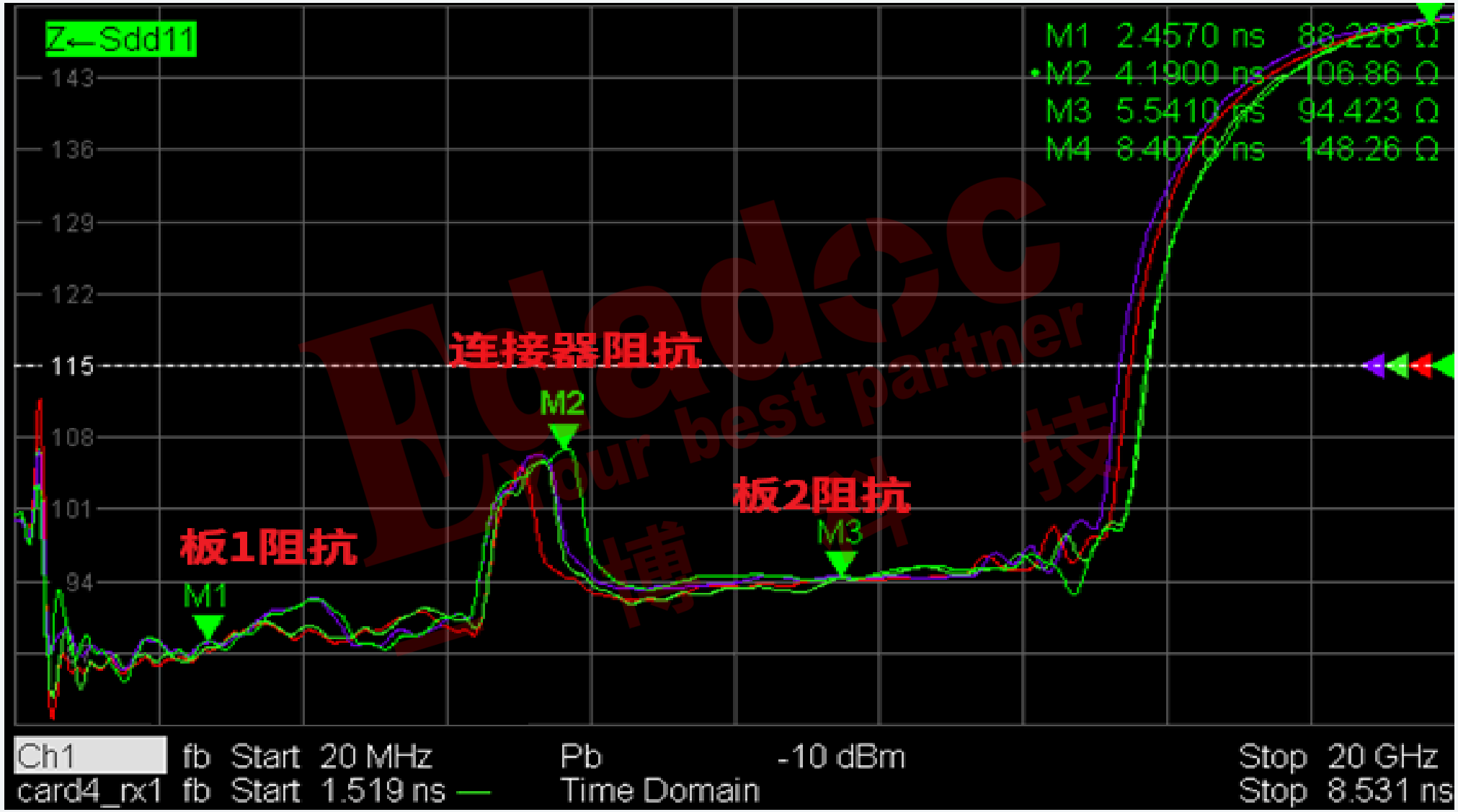
# 另外一个真实案例

- PCIE信号通过连接器连接两块板子



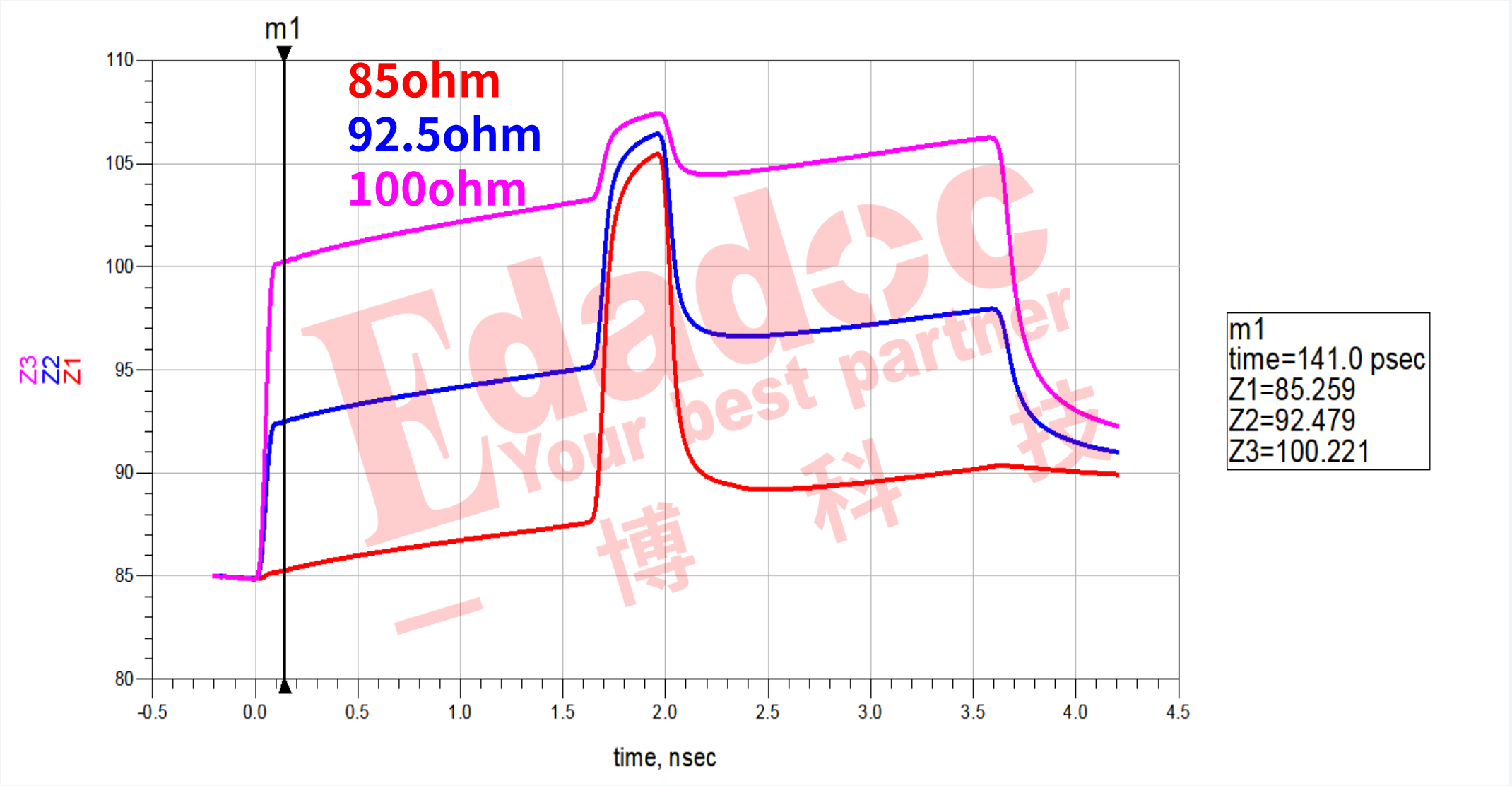
# 另外一个真实案例

- 测试结果：中间连接器阻抗105欧姆

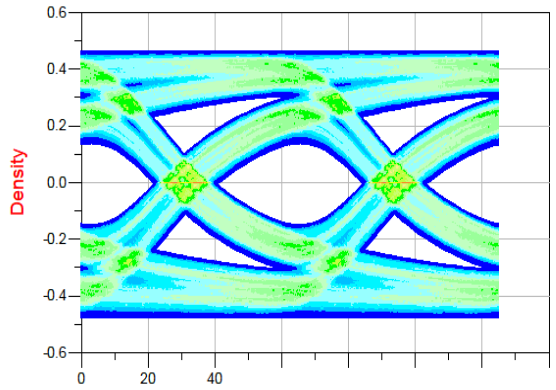


- 连接器阻抗105欧姆，收发芯片内阻85欧姆情况下两块板的传输线阻抗该控制多少欧姆?

- 两块板子分别按照100欧姆，92.5欧姆和85欧姆来控制的全链路阻抗结果

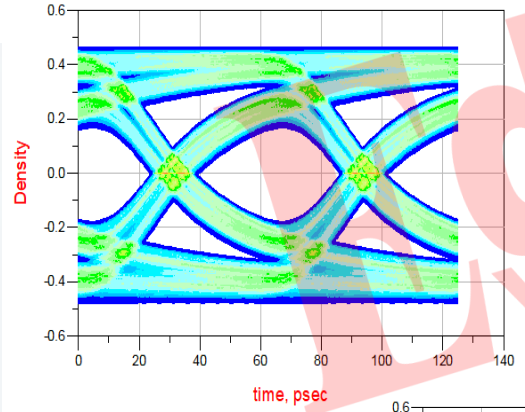


- 不同阻抗下PCIE4.0信号眼图仿真结果对比



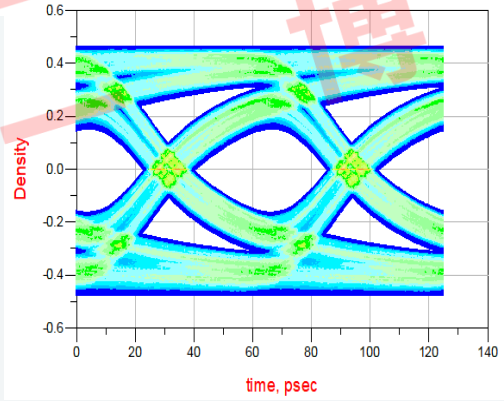

| measurement | Summary |
|---|---|
| Level1 | 0.304 |
| Level0 | -0.303 |
| Height | 0.237 |
| Width | 4.406E-11 |
| WidthAtBER | 1.406E-11 |
| HeightAtBER | 0.033 |

**100欧姆：眼高33mV**




| measurement | Summary |
|---|---|
| Level1 | 0.317 |
| Level0 | -0.317 |
| Height | 0.281 |
| Width | 4.719E-11 |
| WidthAtBER | 2.531E-11 |
| HeightAtBER | 0.116 |

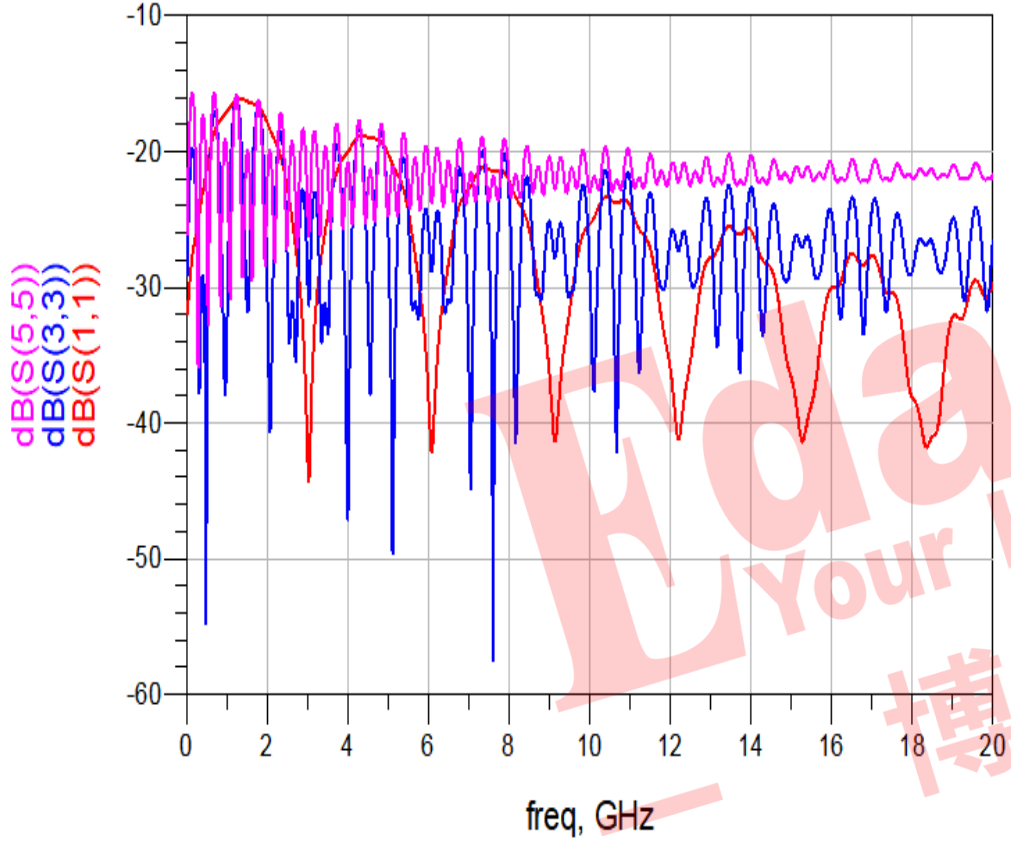
**92.5欧姆：眼高116mV**

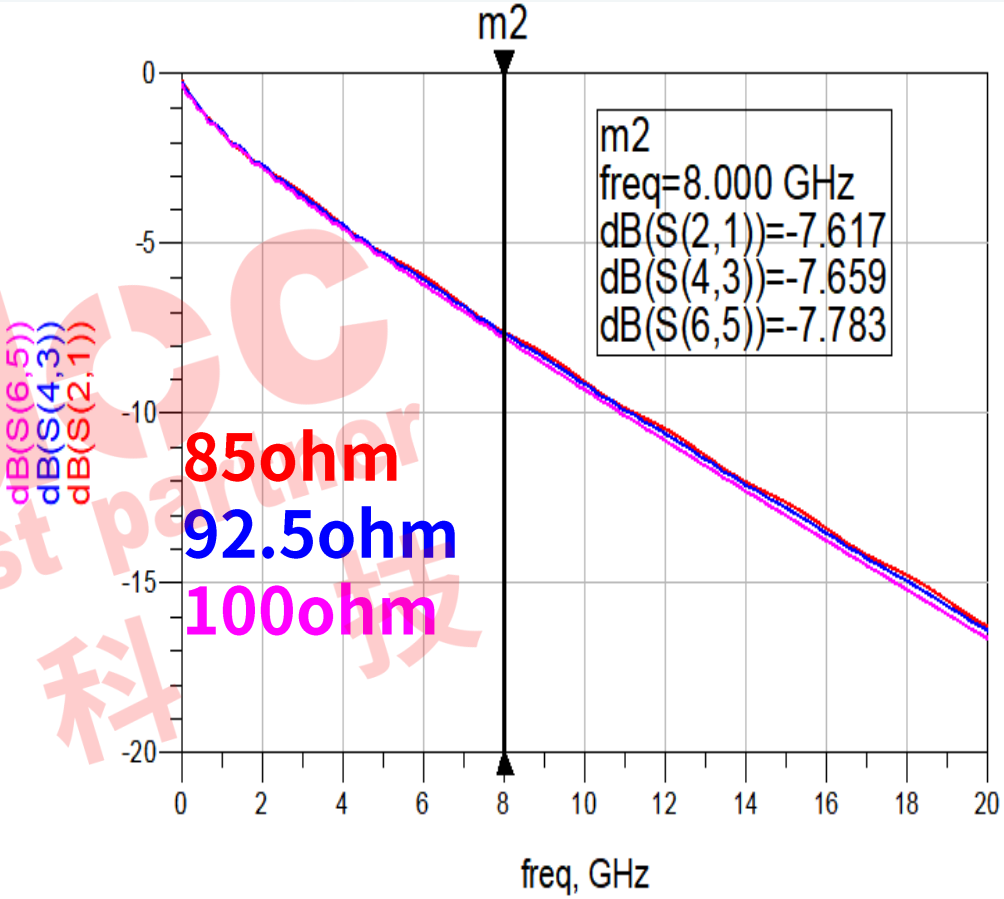



| measurement | Summary |
|---|---|
| Level1 | 0.311 |
| Level0 | -0.310 |
| Height | 0.259 |
| Width | 4.563E-11 |
| WidthAtBER | 2.063E-11 |
| HeightAtBER | 0.075 |

**85欧姆：眼高75mV**

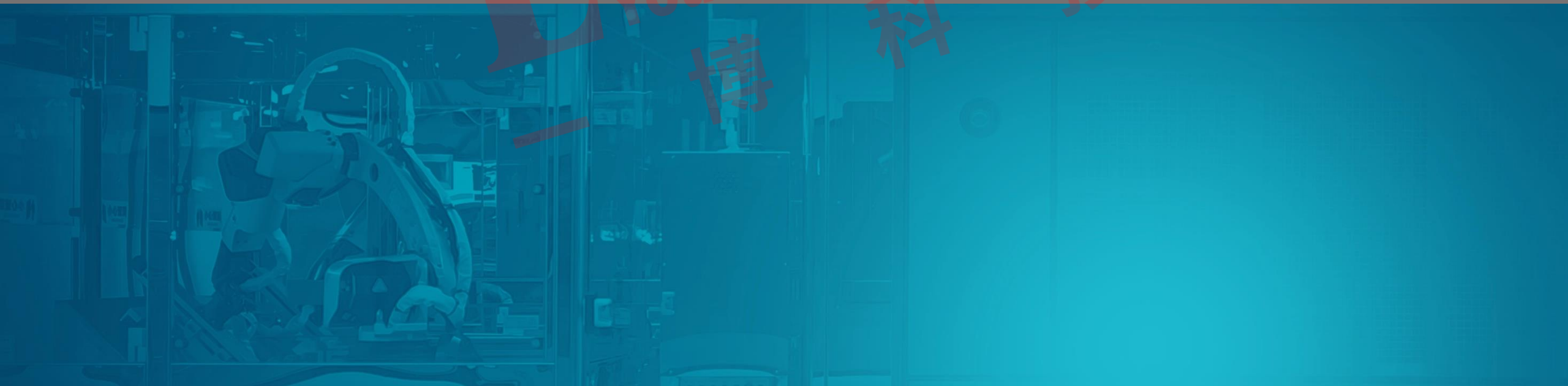
- 从插损回损上找原因



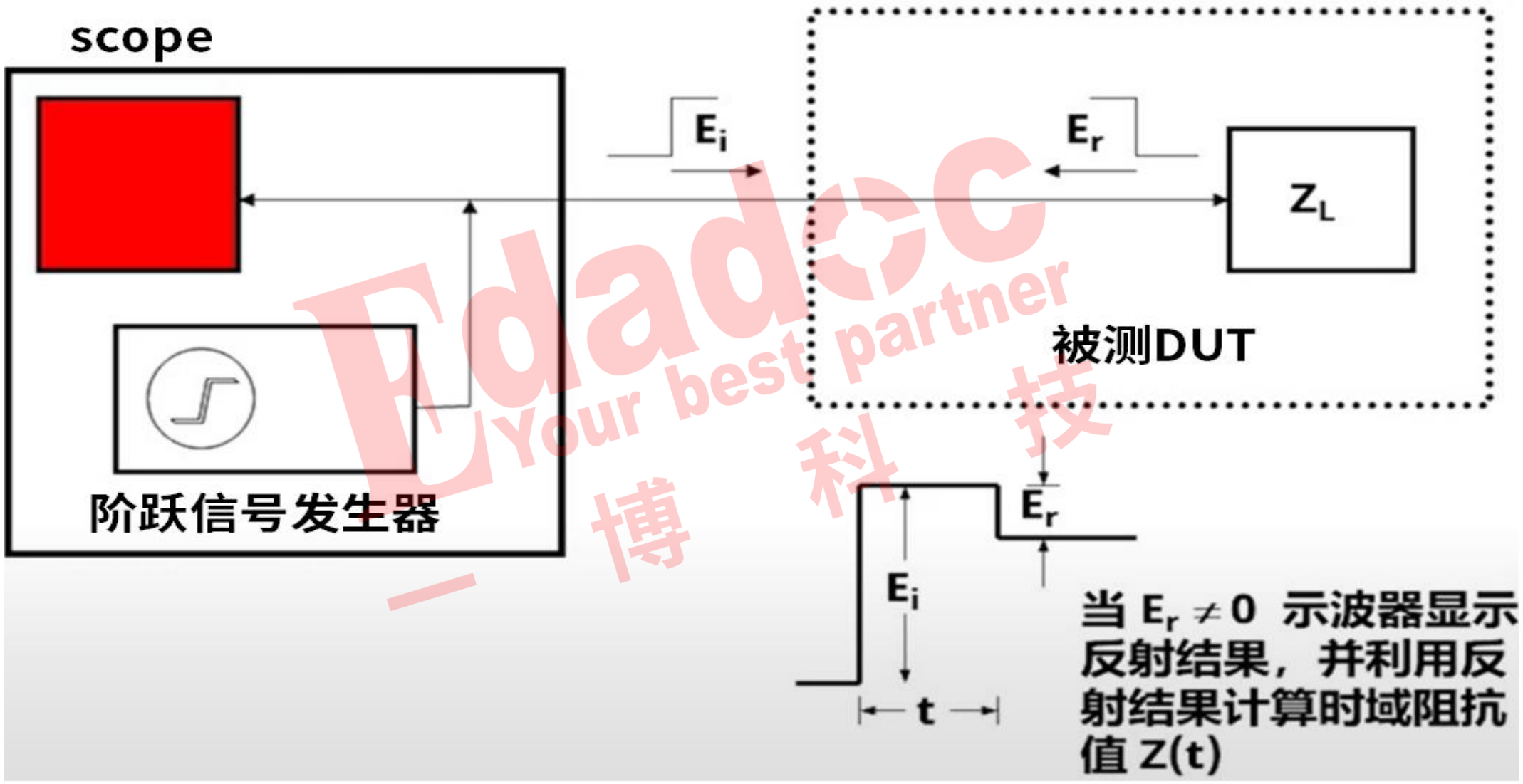



PART 03

# 测出来的阻抗值一定是对的吗？

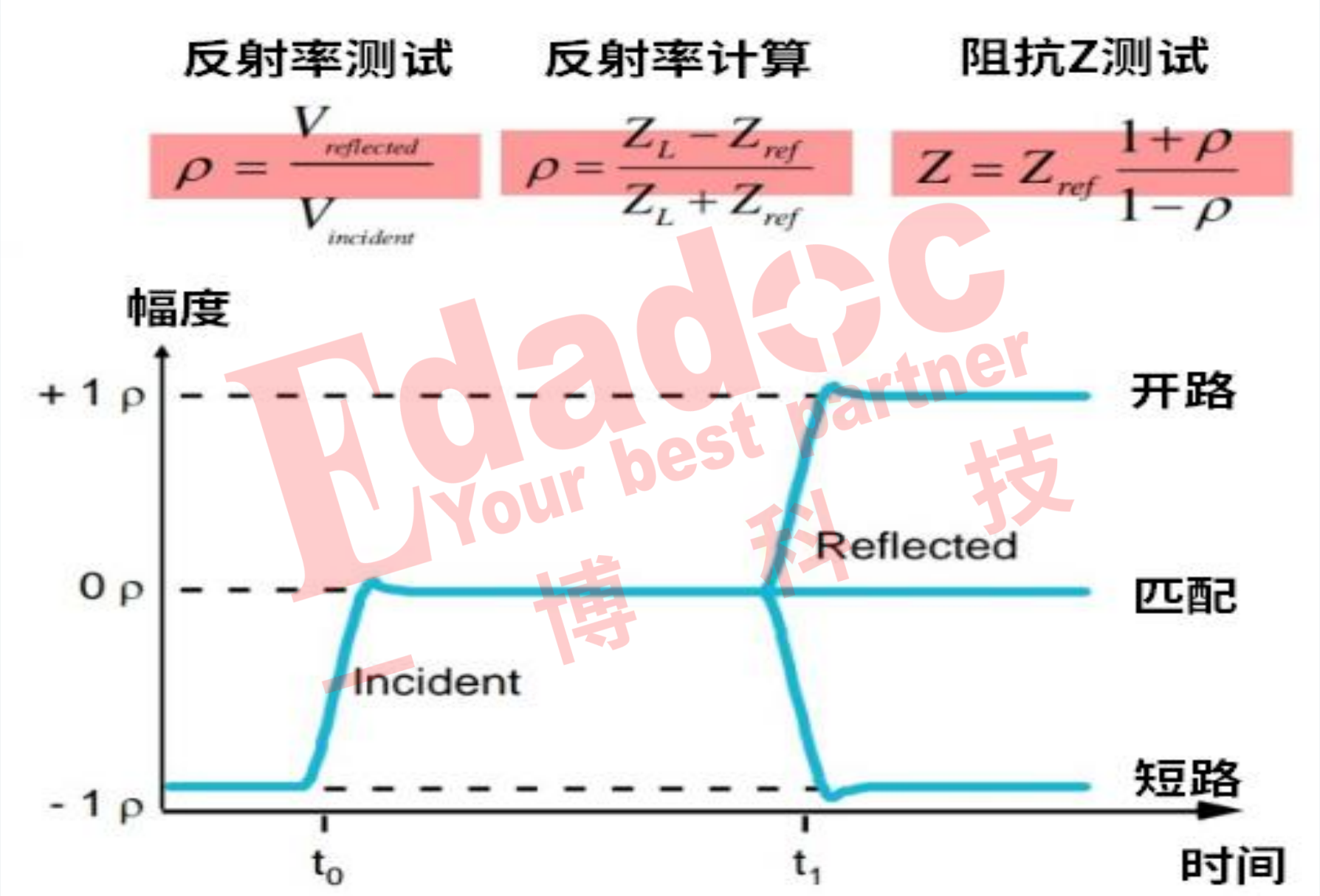


- 时域测试TDR阻抗

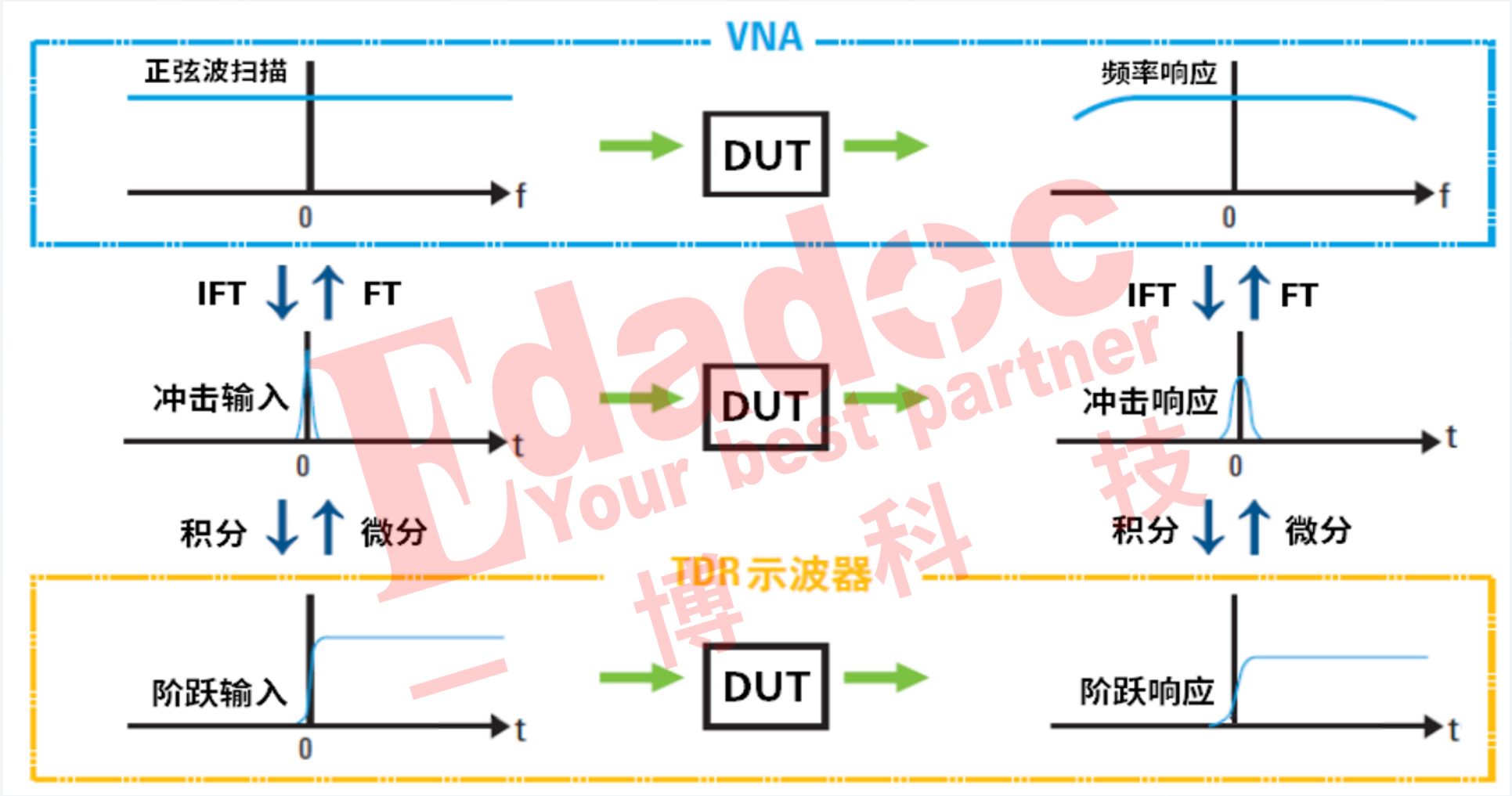


# 阻抗测试的基本原理

- 时域测试TDR阻抗



- 频域测试TDR阻抗---傅里叶逆变换



阻抗测试的“30%~70%”

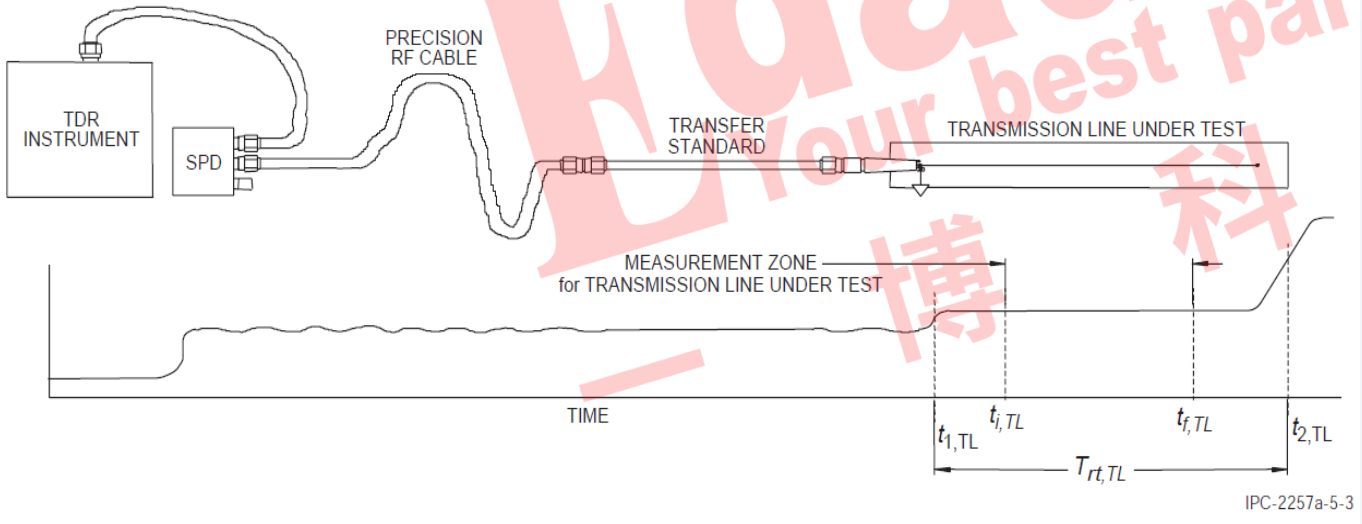
- 出处

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

2215 Sanders Road
Northbrook, IL 60062-6135

# IPC-TM-650
# TEST METHODS MANUAL

| Number | |
|---|---|
| **2.5.5.7** | |
| Subject | |
| **Characteristic Impedance of Lines on Printed Boards by TDR** | |
| Date | Revision |
| **03/04** | **A** |
| Originating Task Group | |
| **TDR Test Method Task Group (D-24a)** | |



IPC-2257a-5-3

*Step 4* – Determine the initial instant, $t_{i,TL}$, of measurement zone (see Figure 5-3) using:

$$t_{i,TL} = t_{1,TL} + x_{i\%} T_{rt,TL}$$

where $x_{i\%}$ is the lower limit of the measurement zone and is 30 % unless otherwise specified by the user.

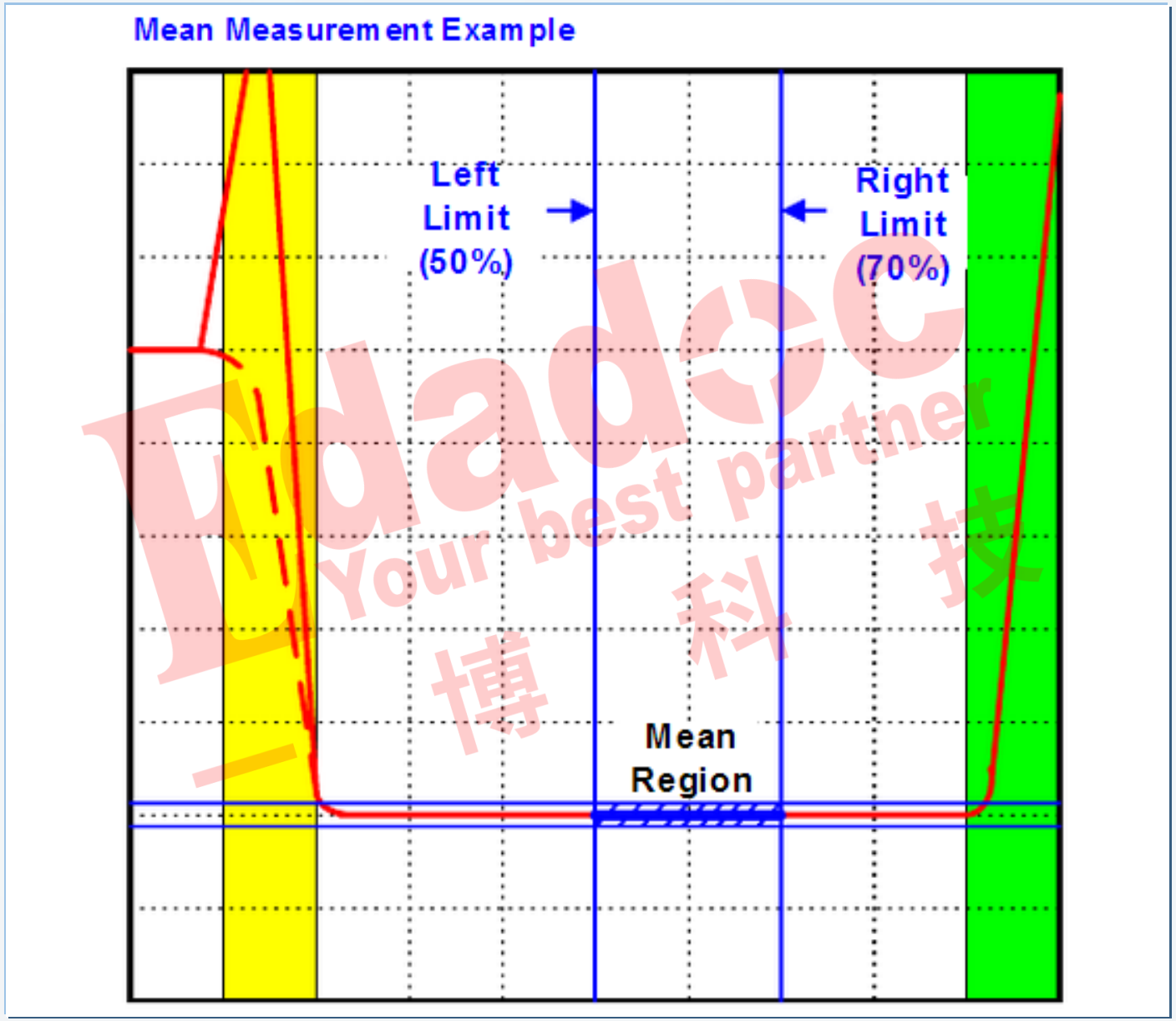
*Step 5* – Determine final instant, $t_{f,TL}$, of measurement zone (see Figure 5-3) using:

$$t_{f,TL} = t_{1,TL} + x_{f\%} T_{rt,TL}$$

where $x_{f\%}$ is the upper limit of the measurement zone and is 70 % unless otherwise specified by the user.

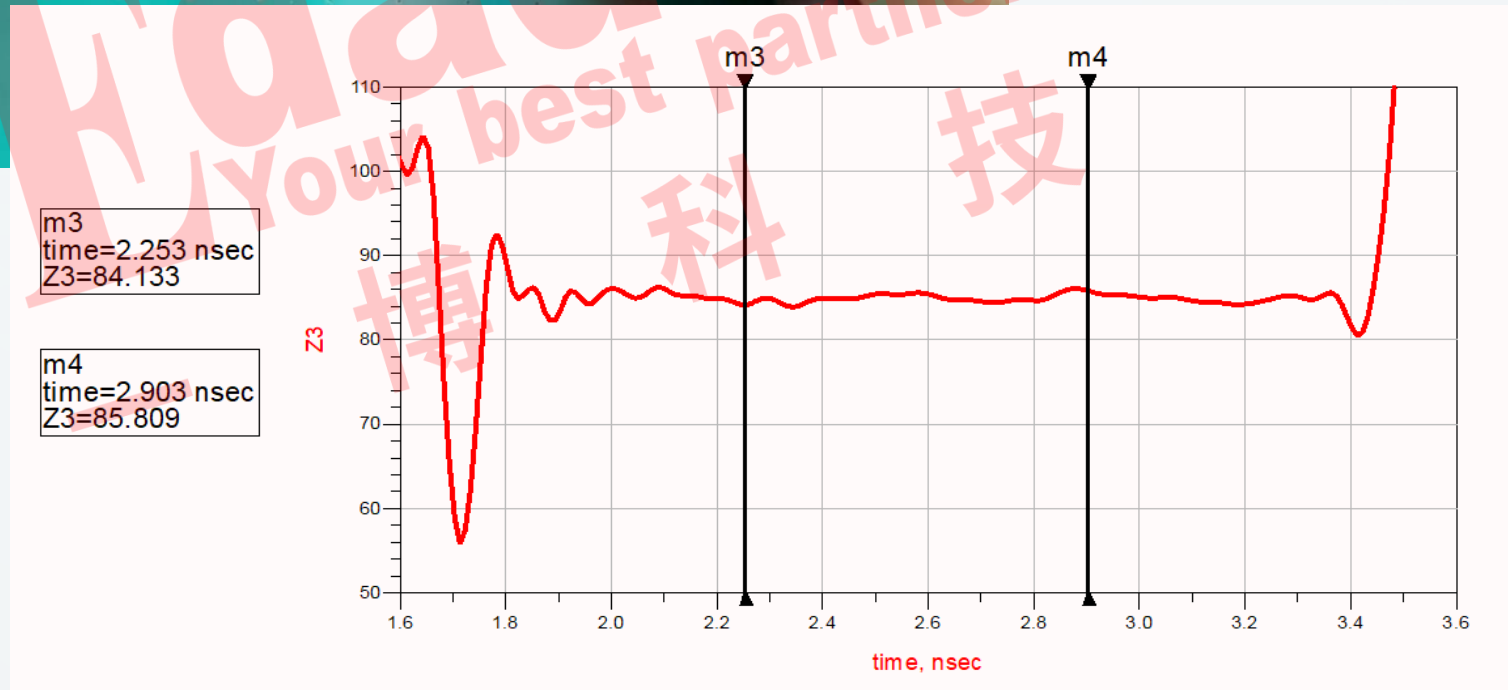
# Intel及多数板厂阻抗测试标准

- Intel及多数板厂阻抗测试标准：50%-70%



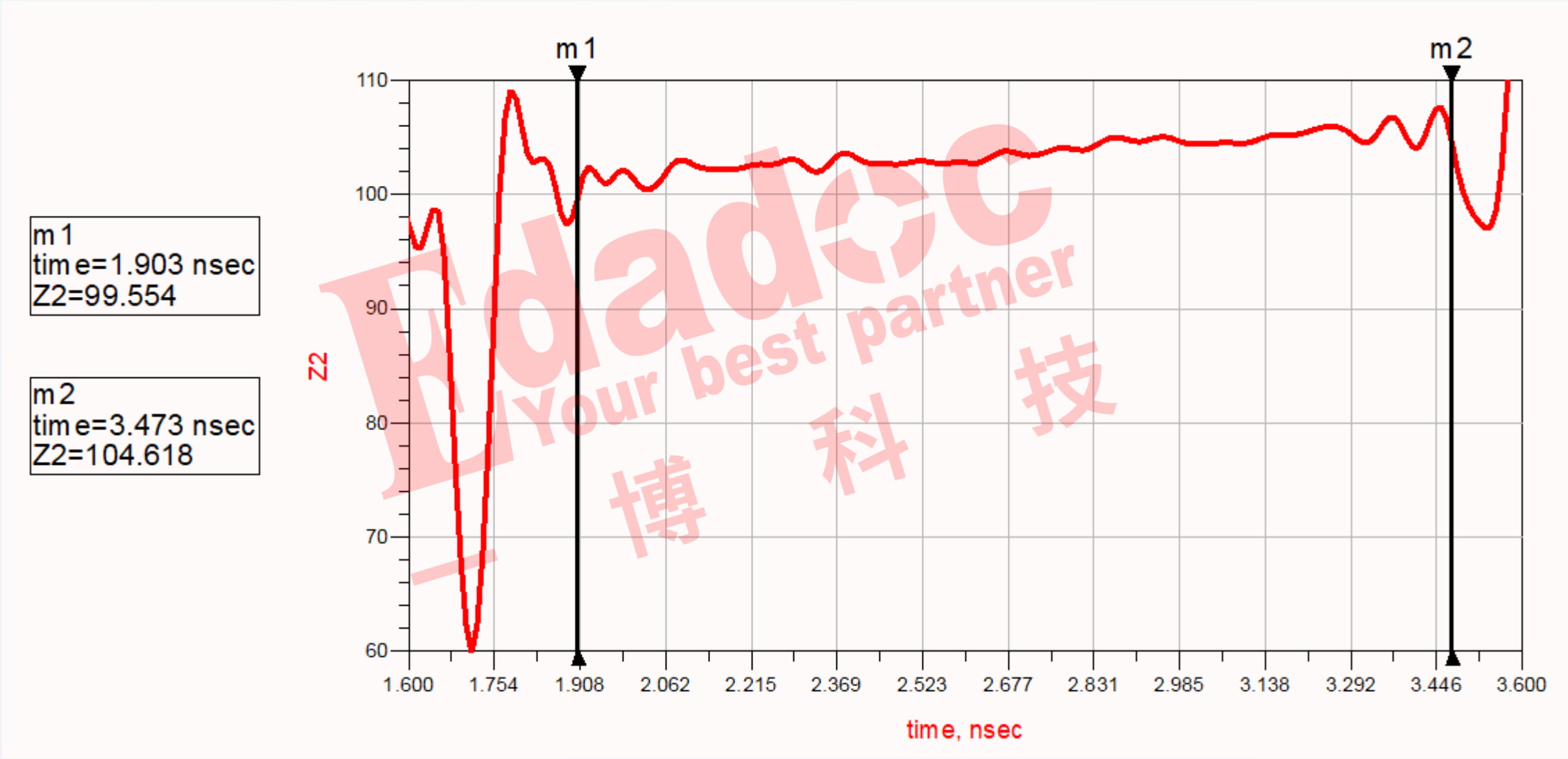
# 阻抗测试看的区域

- 30%-70%区间的测试结果



# 阻抗上漂效应

- 阻抗上漂 100欧姆内层走线 30%-70%区间的阻抗
- 阻抗上漂 100欧姆的内层走线 起始到末端，相差5.1欧姆

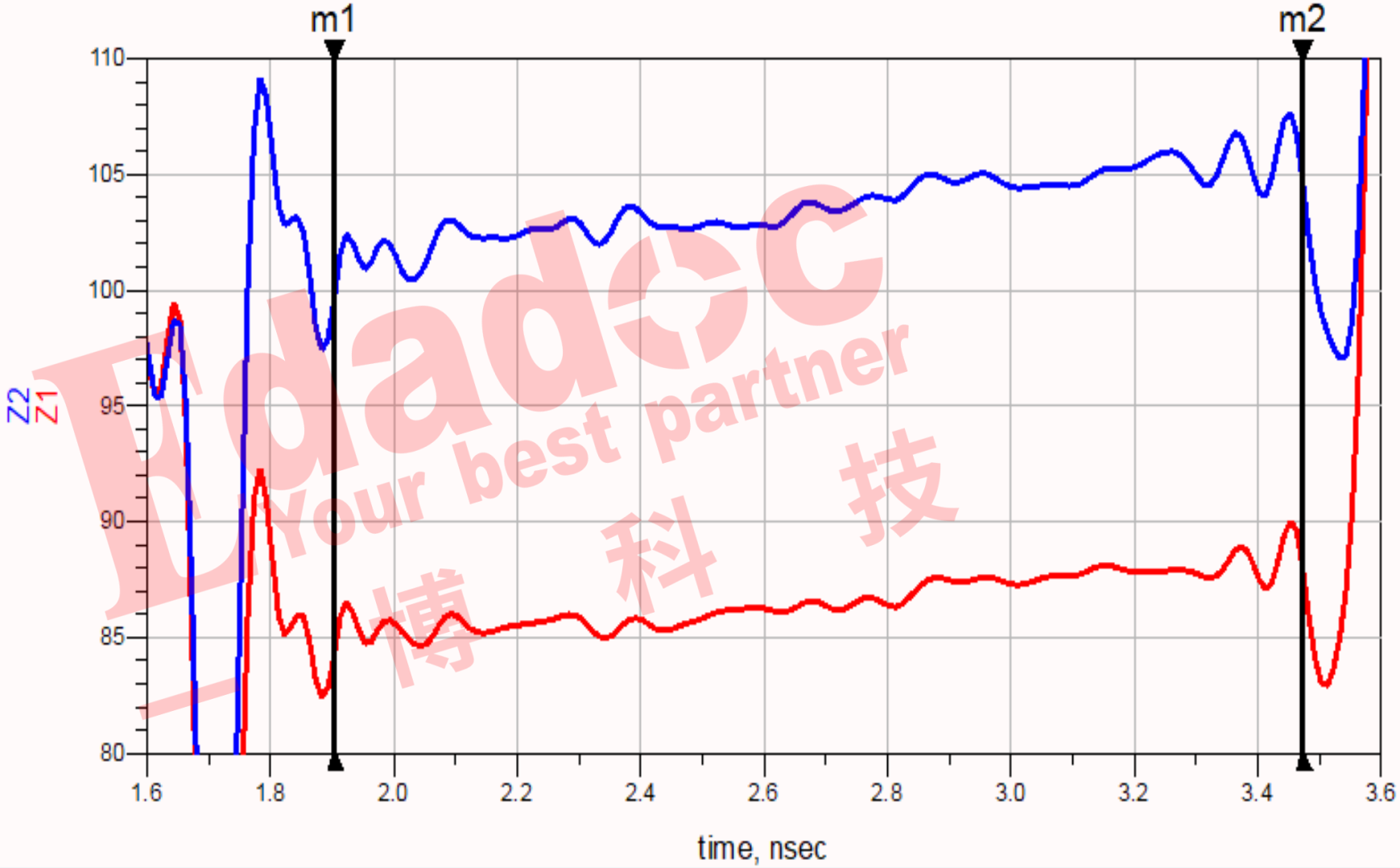


# 阻抗上漂效应

- 阻抗上漂 对比 85欧姆阻抗上漂3.8ohm，100欧姆阻抗上漂5.1ohm。

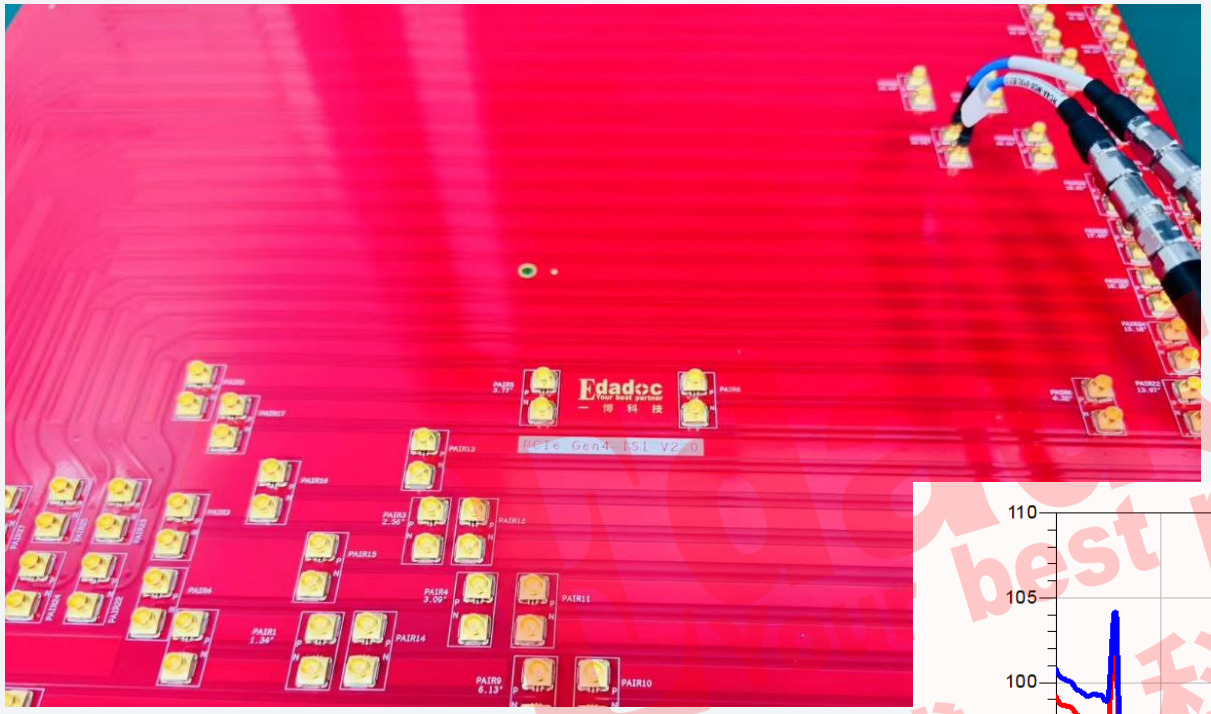
m1
time=1.903 nsec
Z1=84.213
Z2=99.554

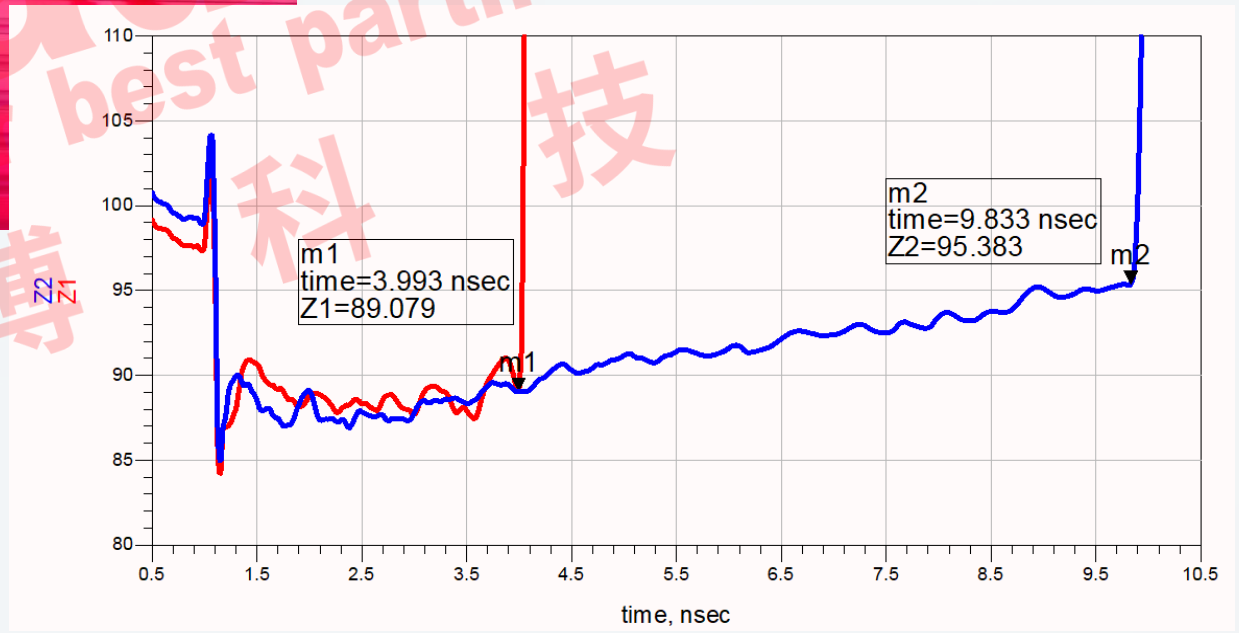
m2
time=3.473 nsec
Z1=87.982
Z2=104.618



# 阻抗上漂效应

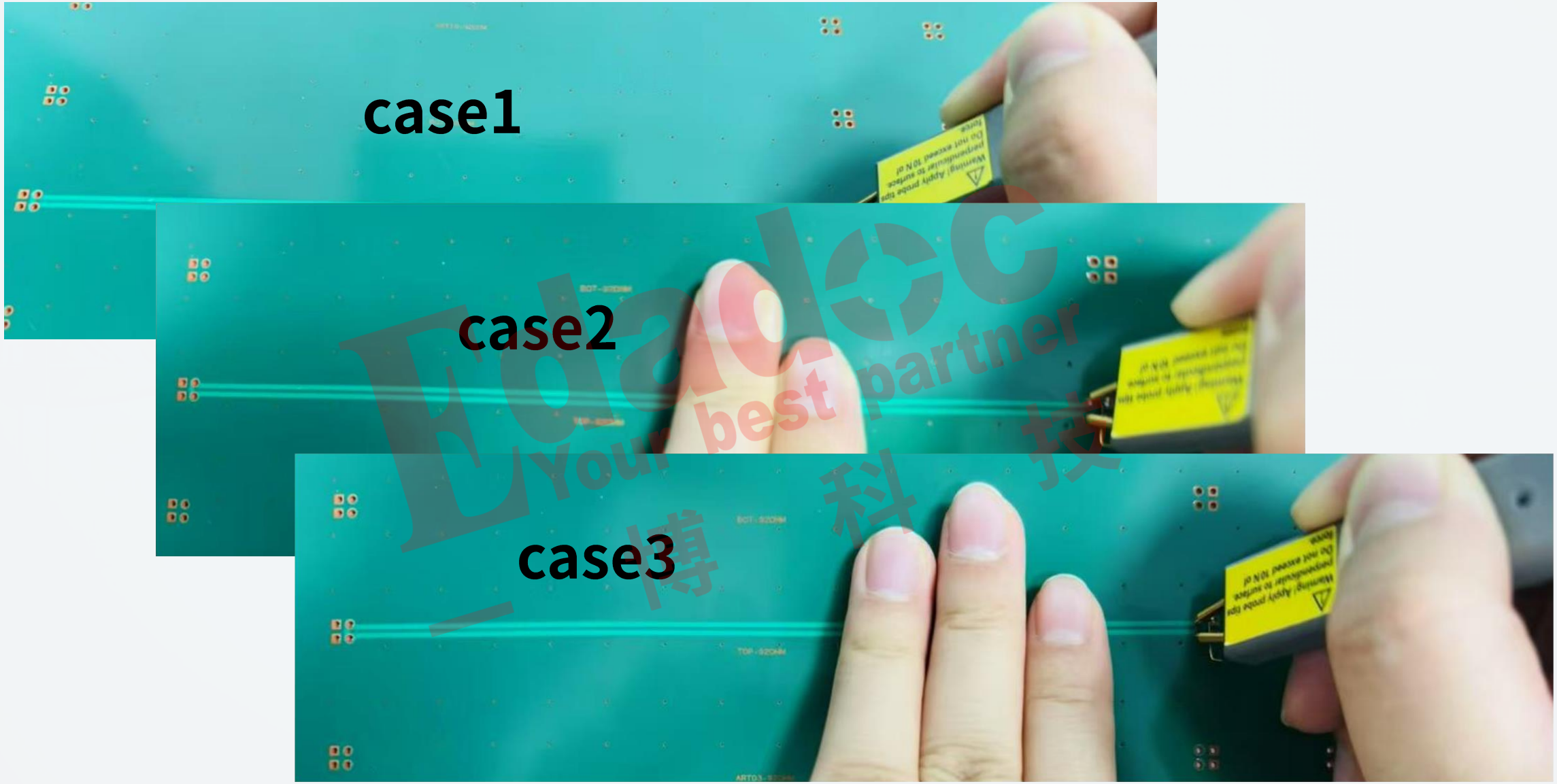
- 不同长度的通道对比，上漂量之间的差异。



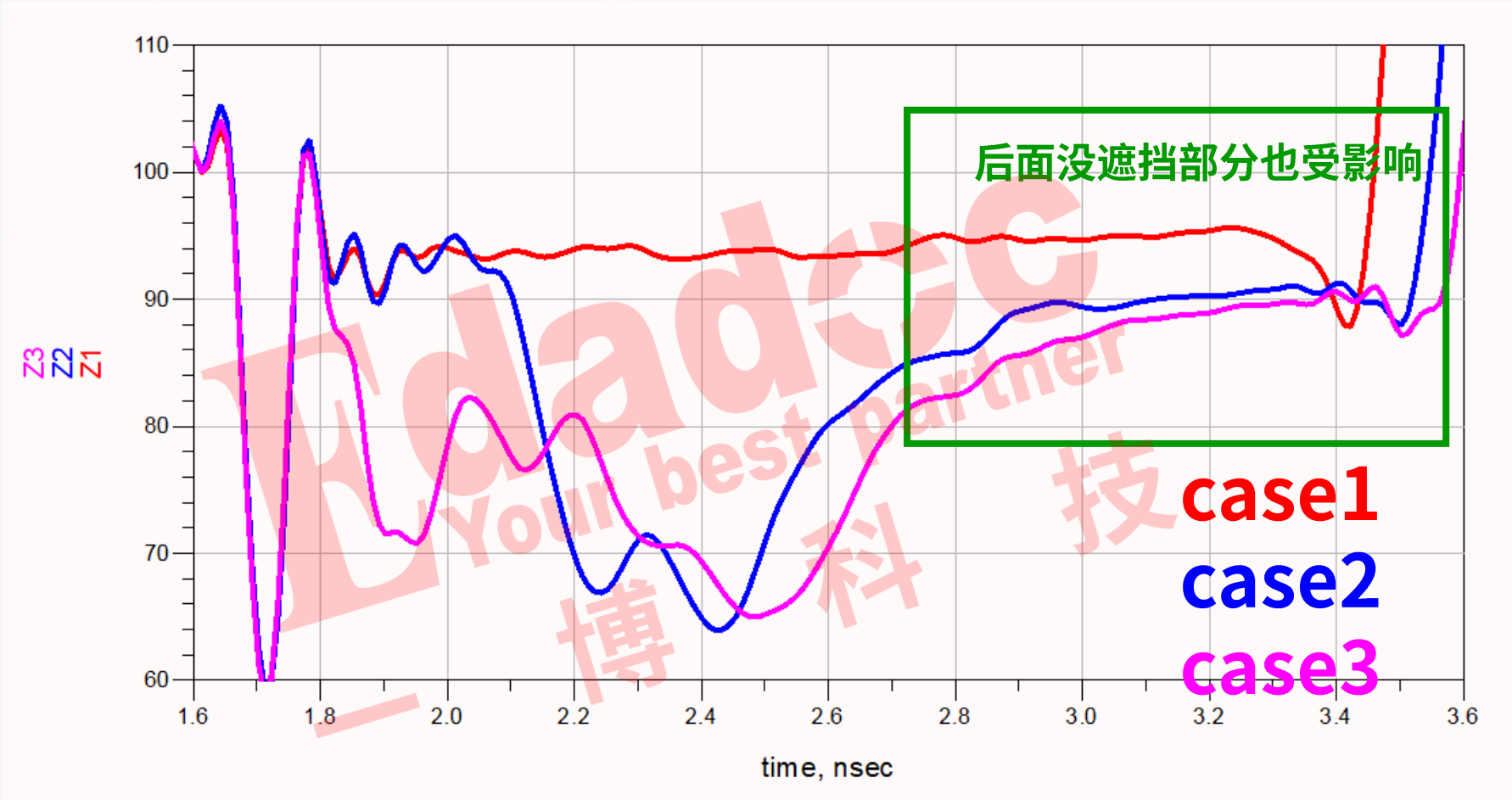



# 阻抗的遮挡效应

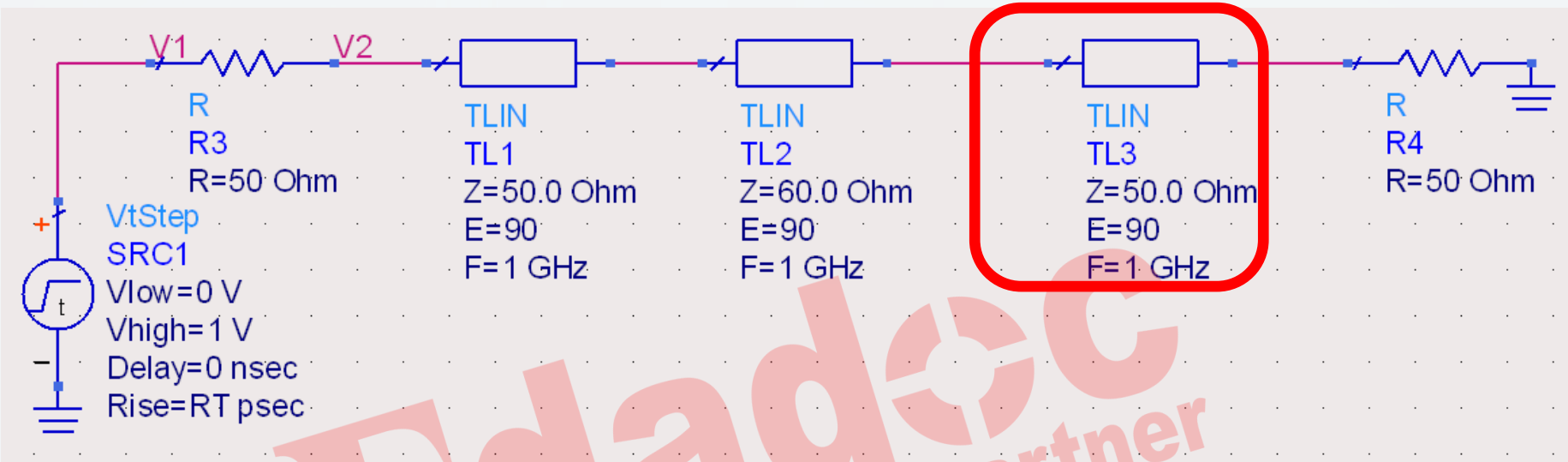
- 一个小实验



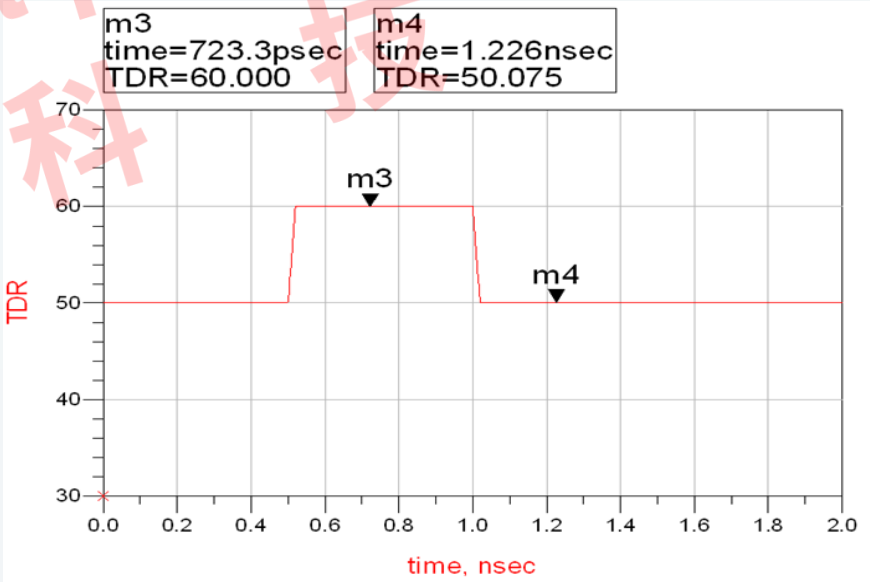
# 阻抗的遮挡效应



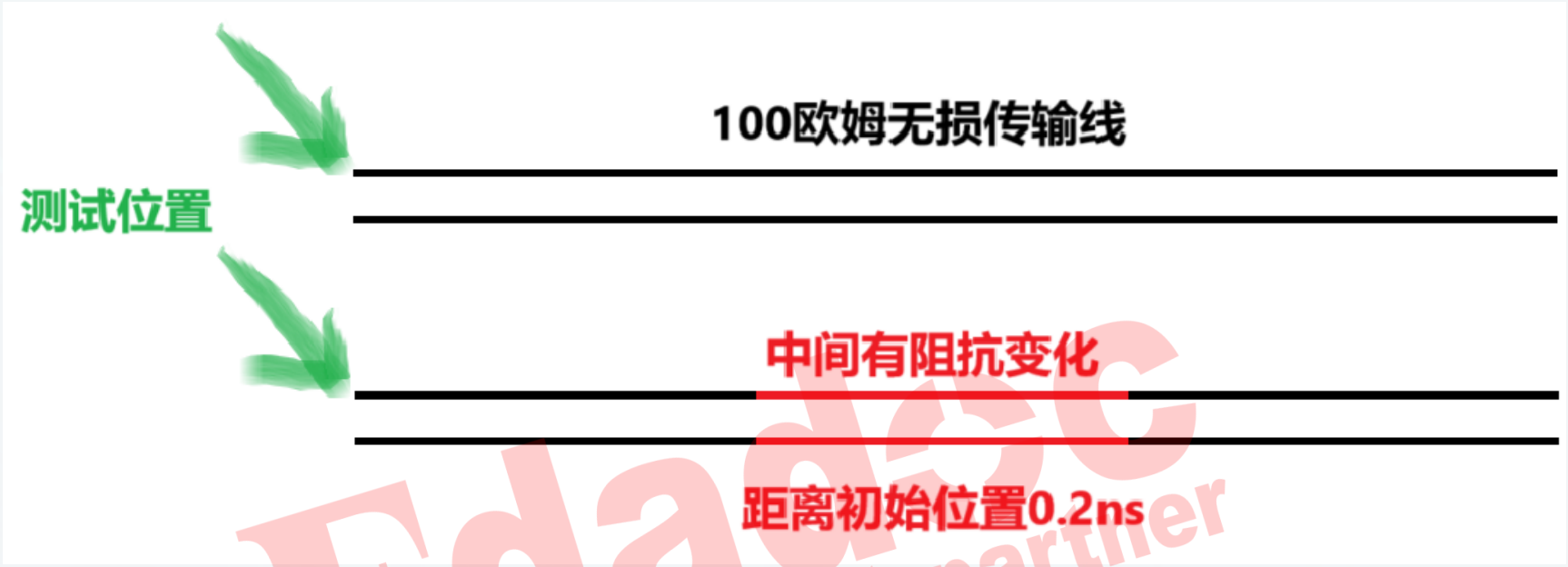
# 阻抗的遮挡效应的理论验证

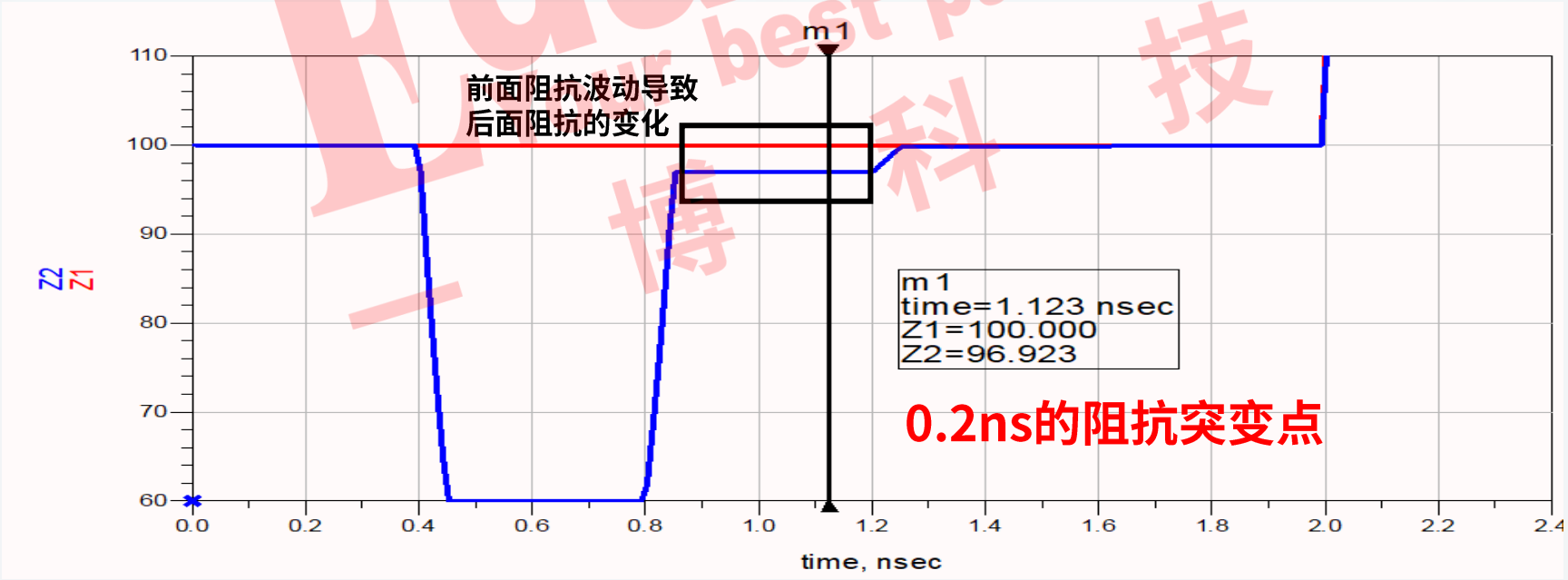



第一次反射1/11，剩下10/11传输
第二次反射系数(50-60)/(60+50)
反射10/11的-1/11，也就是-10/121
而这个经过第一次阻抗变化的地方时，又会反射掉-10/121的-1/11，传输12/11
实际再传向源端的等于-10/121*12/11=-120/1331
这时候V2变化了1/11-120/1331=1/1331
所以本来应该是50欧姆的阻抗，变成了50*1332/1330=50.075

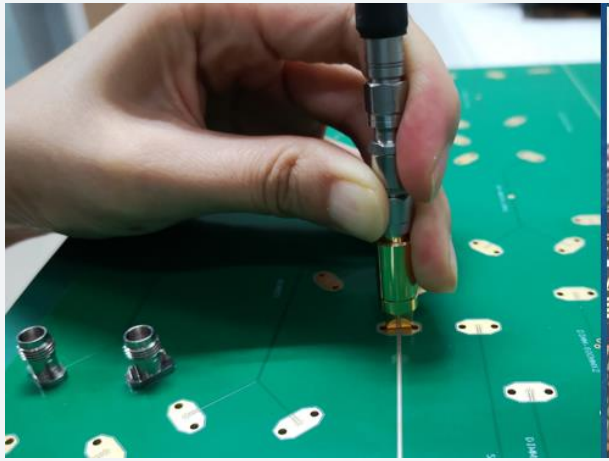


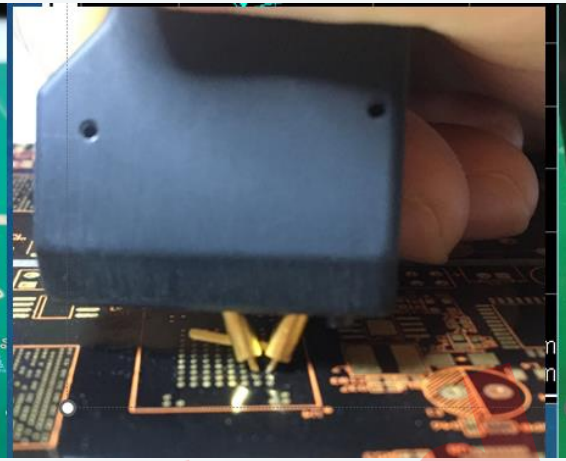
# 阻抗的遮挡效应仿真验证

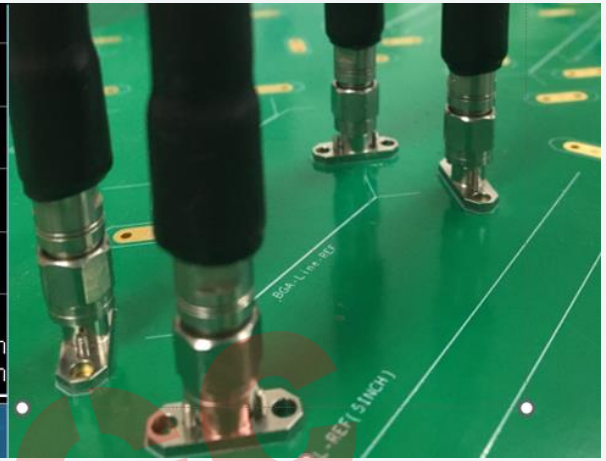


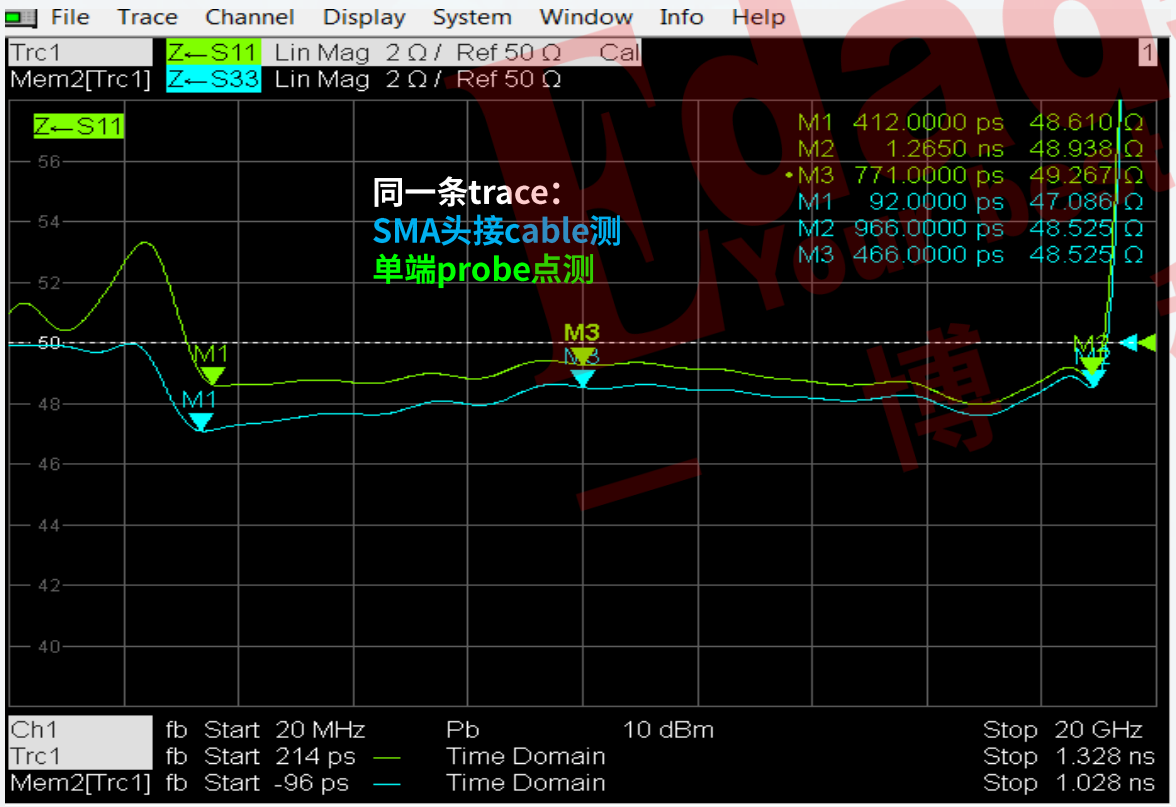



# 点测探头也是一种遮挡效应



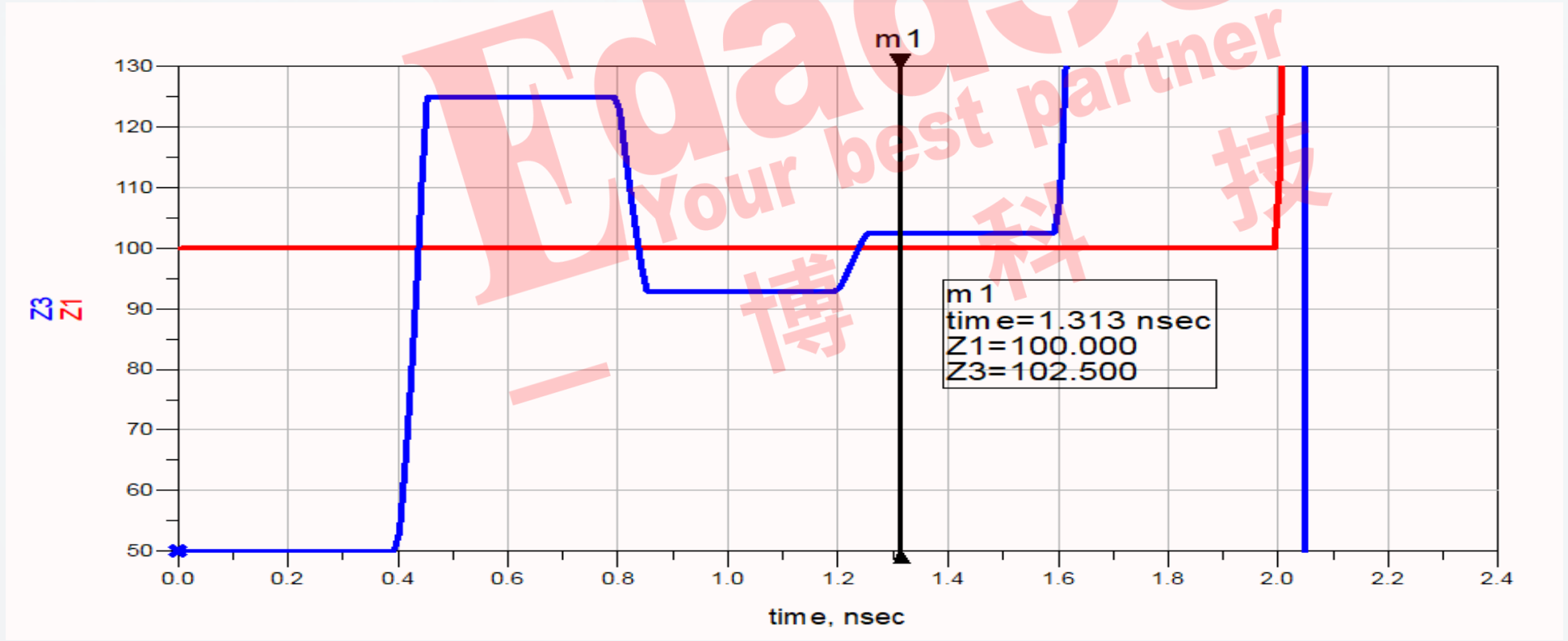






# 另外一种遮挡效应

- 如果不在发送端测试，在链路的中间测试……

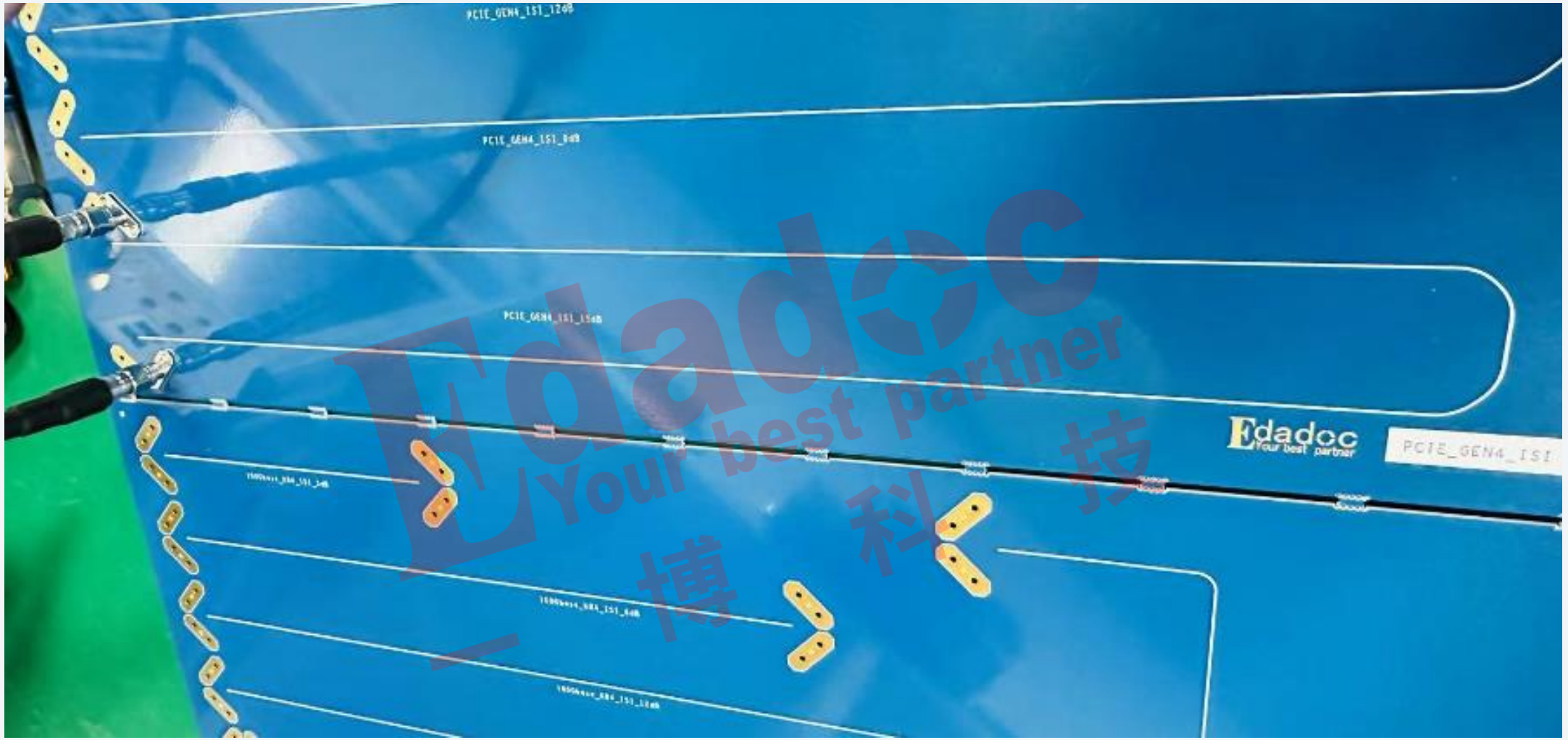



# 另外一种遮挡效应

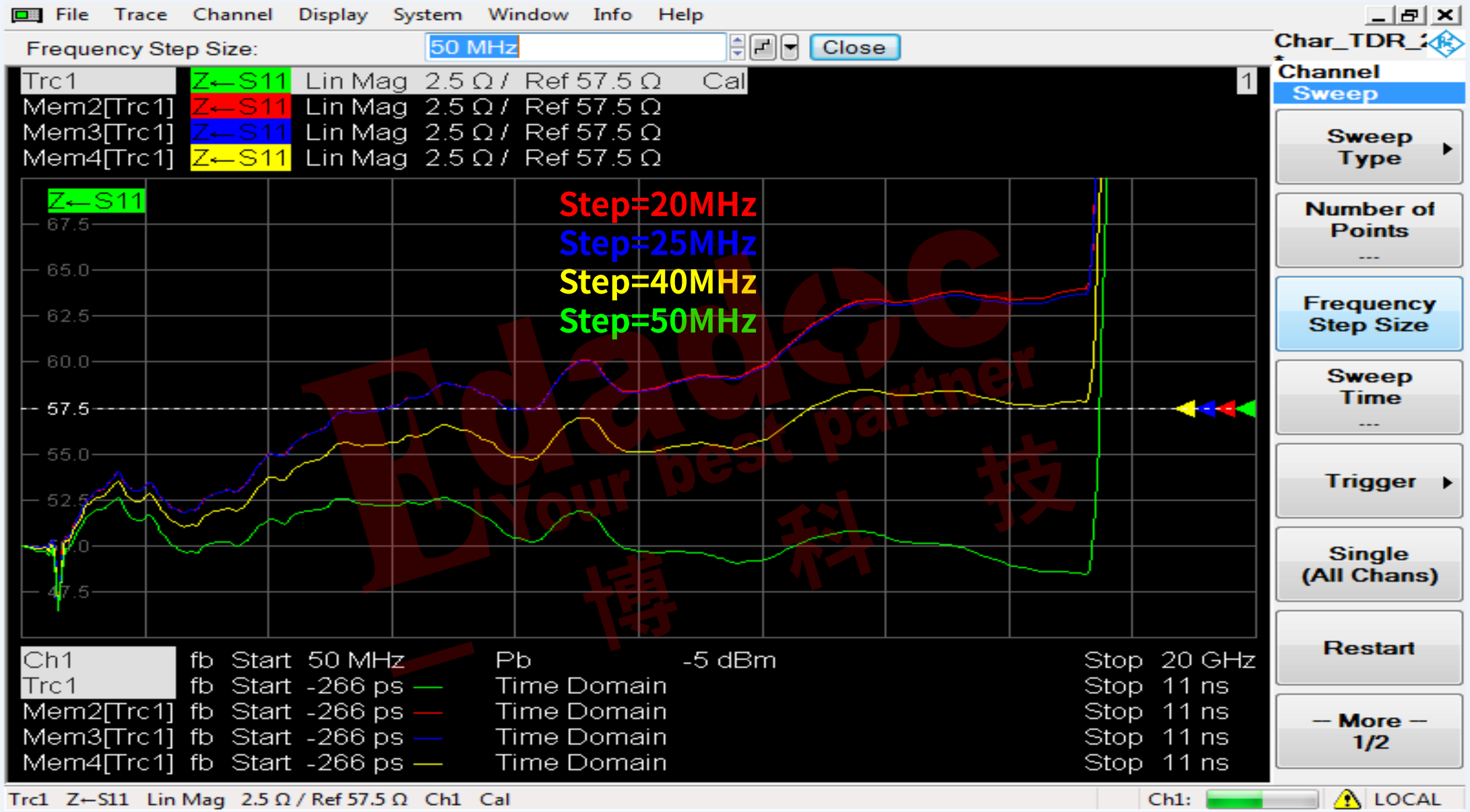
- 实测也是这样的现象。。。

# Step也会影响阻抗？

- 网络分析仪设置频率间隔step也会影响测出来的阻抗？？？



# Step也会影响阻抗？

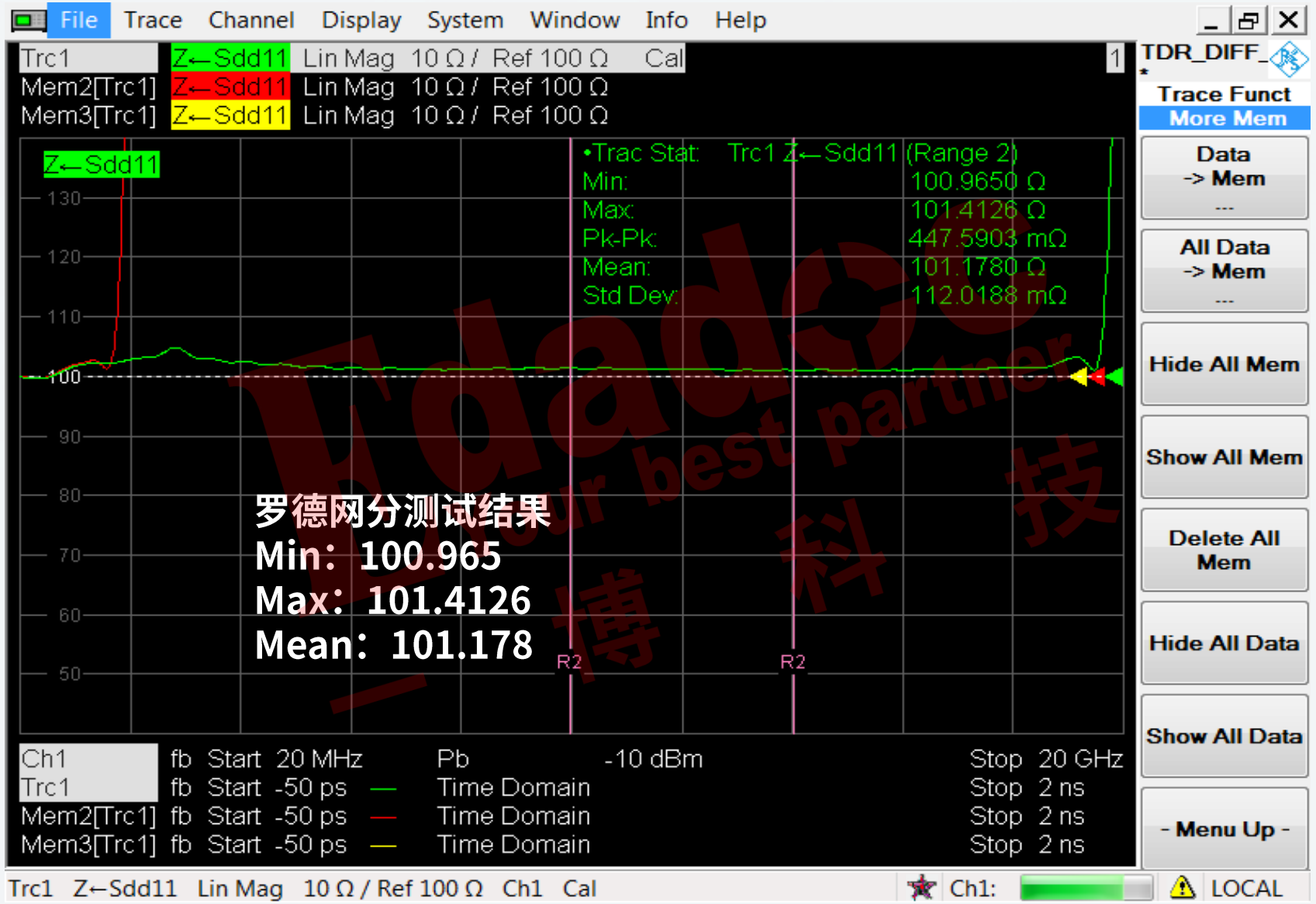


# 阻抗的不同测试仪器之间的偏差

- 用不同测试仪器对号称阻抗很理想的空气棒进行阻抗测试

# 阻抗的不同测试仪器之间的偏差

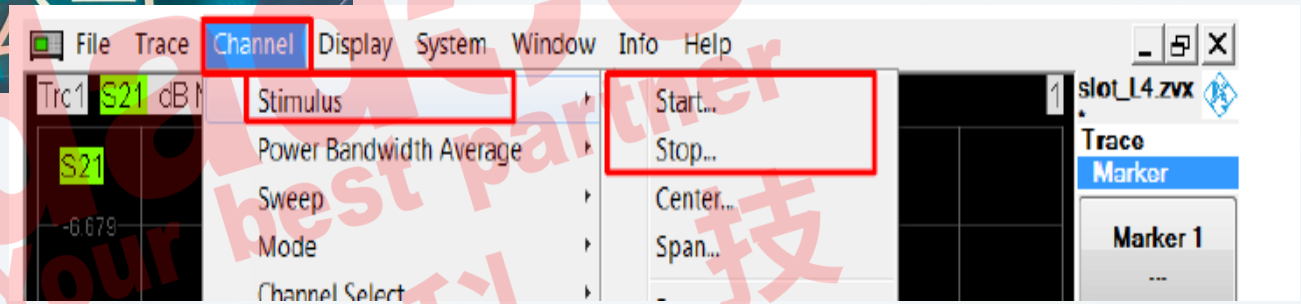
- 用不同测试仪器对号称阻抗很理想的空气棒进行阻抗测试

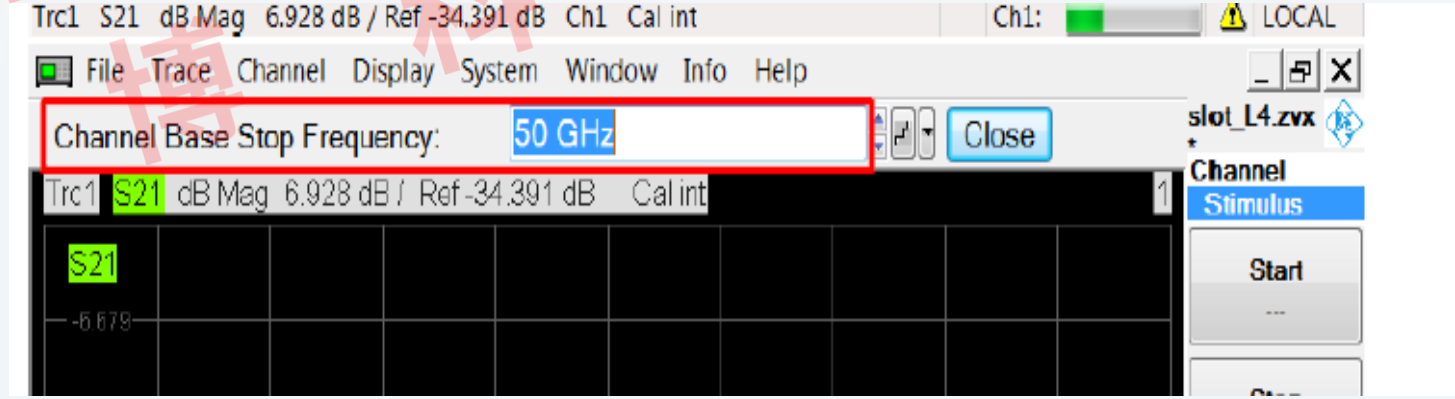


# 阻抗的不同测试仪器之间的偏差

- 用不同测试仪器对号称阻抗很理想的空气棒进行阻抗测试

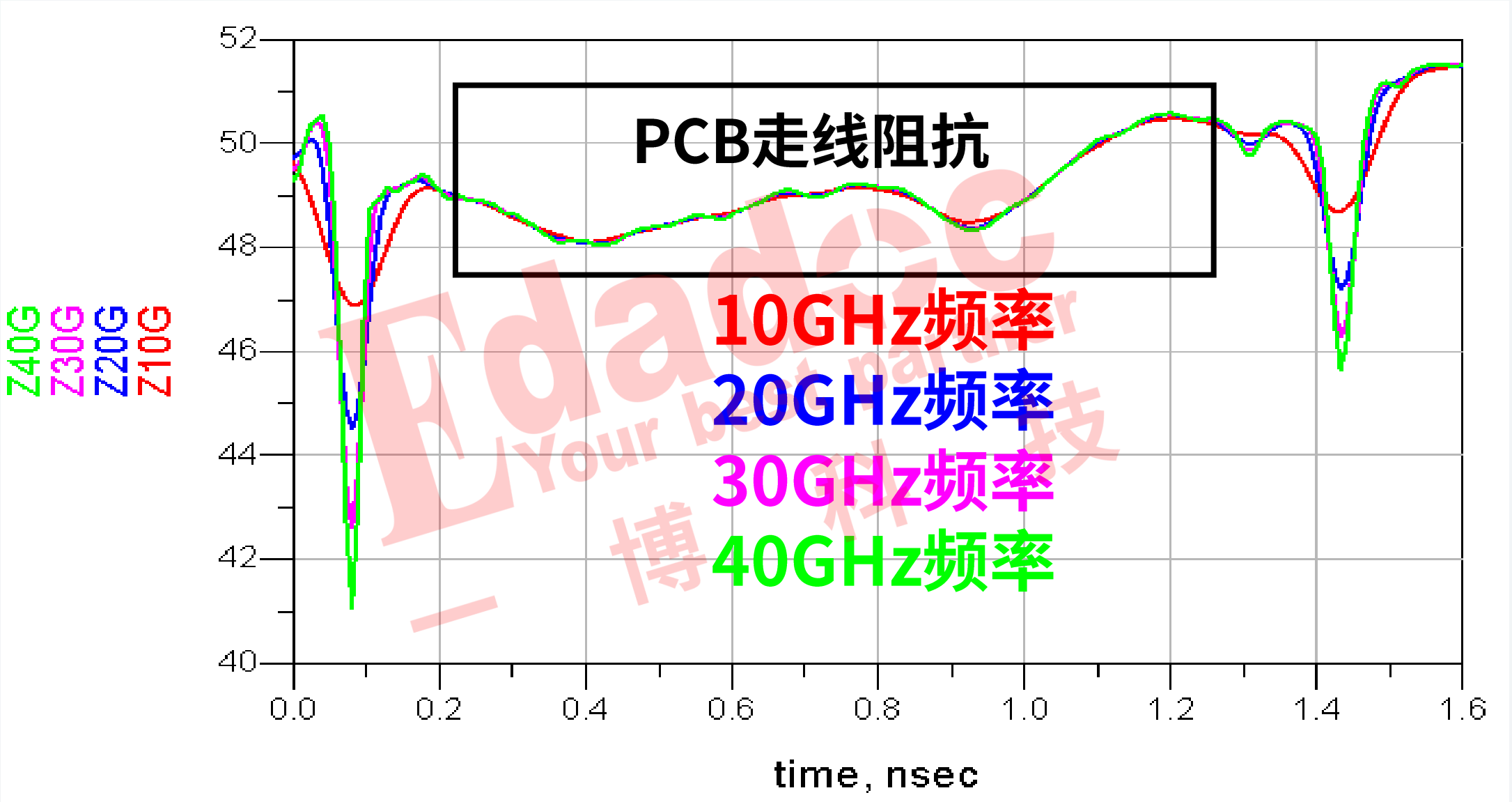

- 一定要用到40GHz以上的网络分析仪来测走线的阻抗?

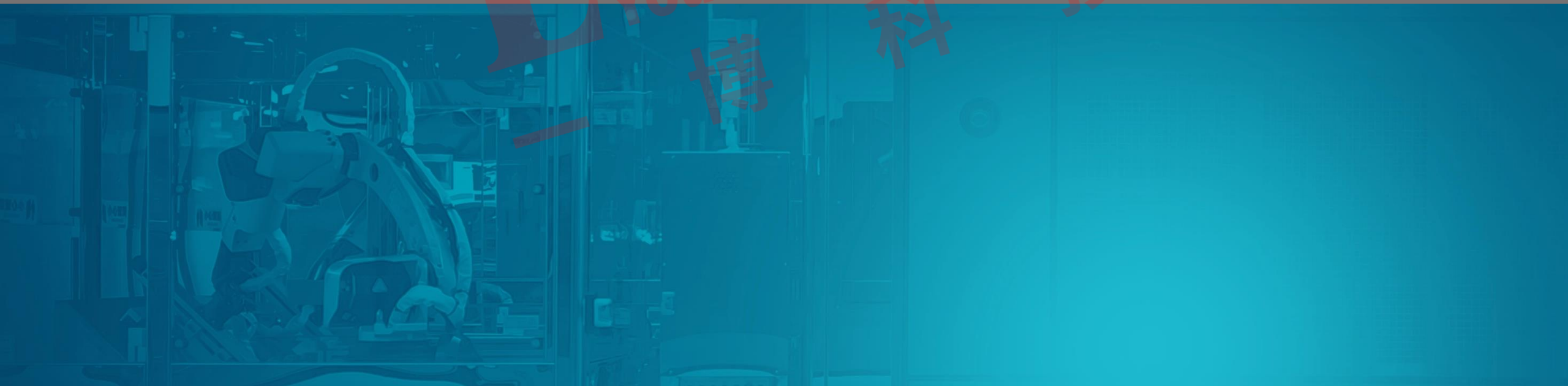
# 测走线阻抗需要用很高的带宽吗？

- 一定要用到40GHz以上的网络分析仪来测走线的阻抗？

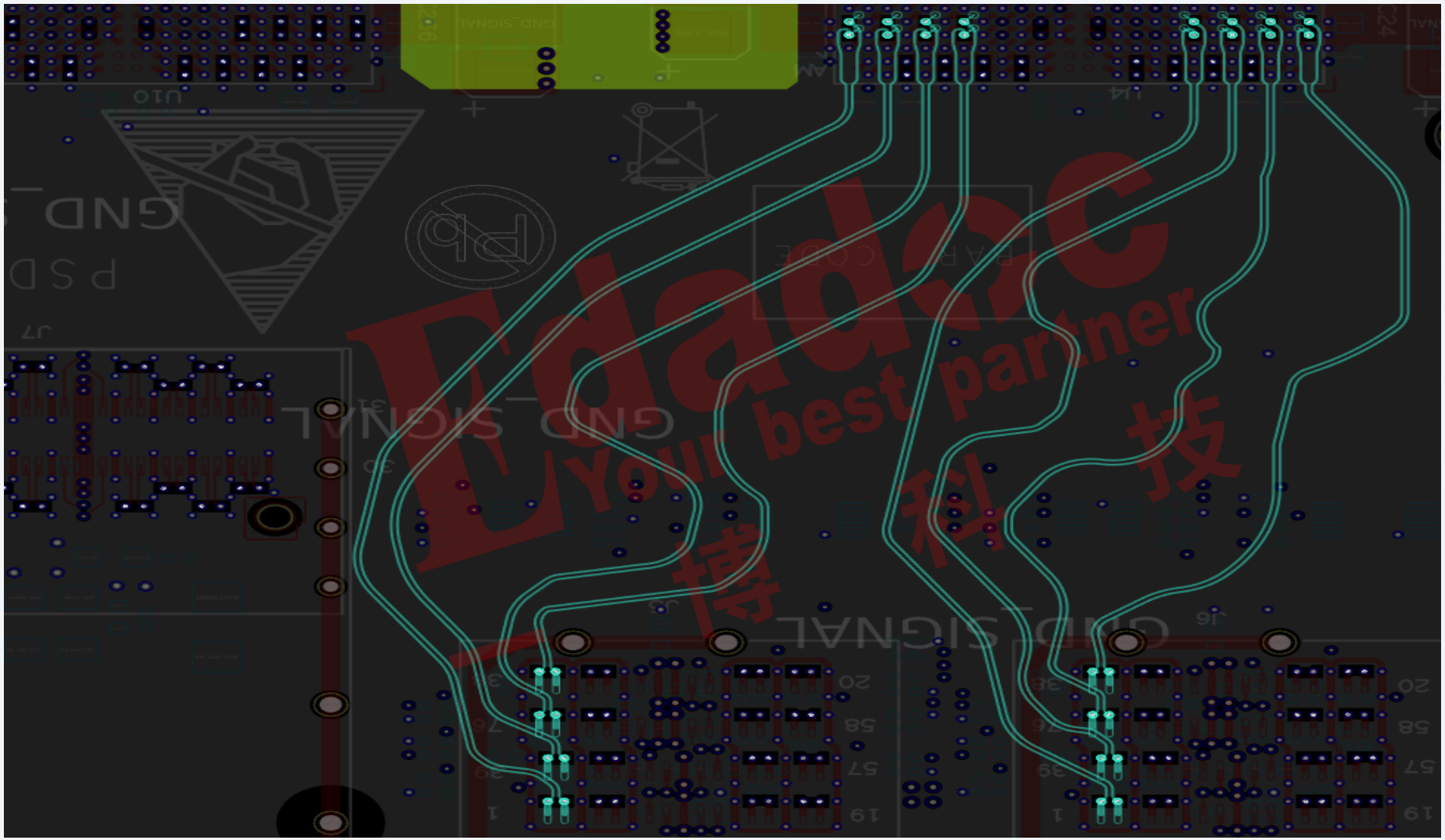


PART 04

# 超高速对阻抗设计和加工同时考验

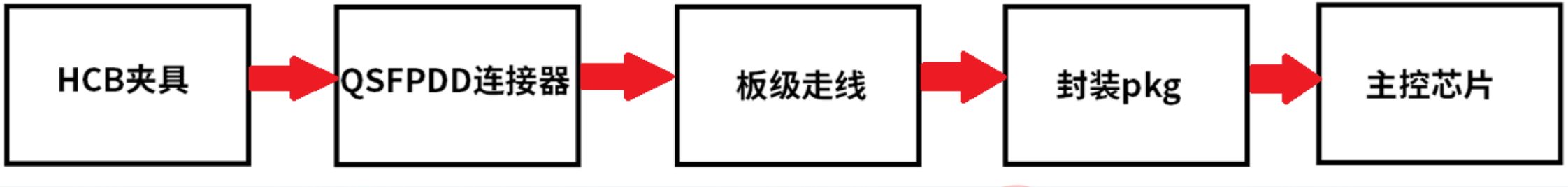


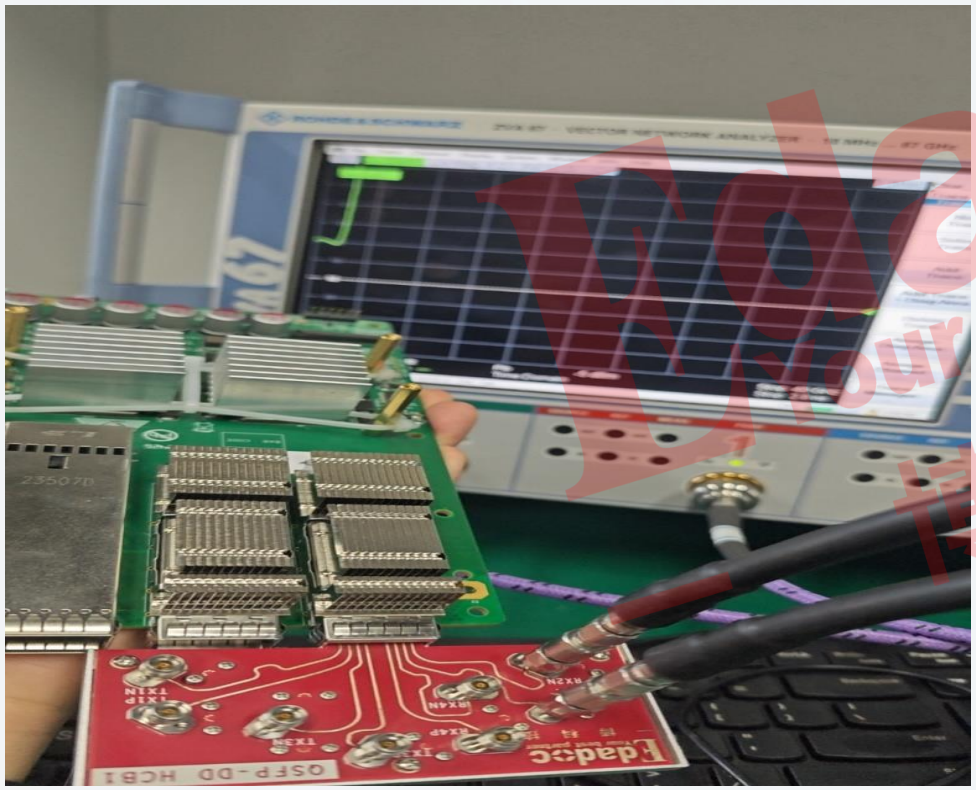
- 第一版客户反馈功能ok，但希望回环的误码率（当前1E-7）再降低一点。
- PCB链路如下

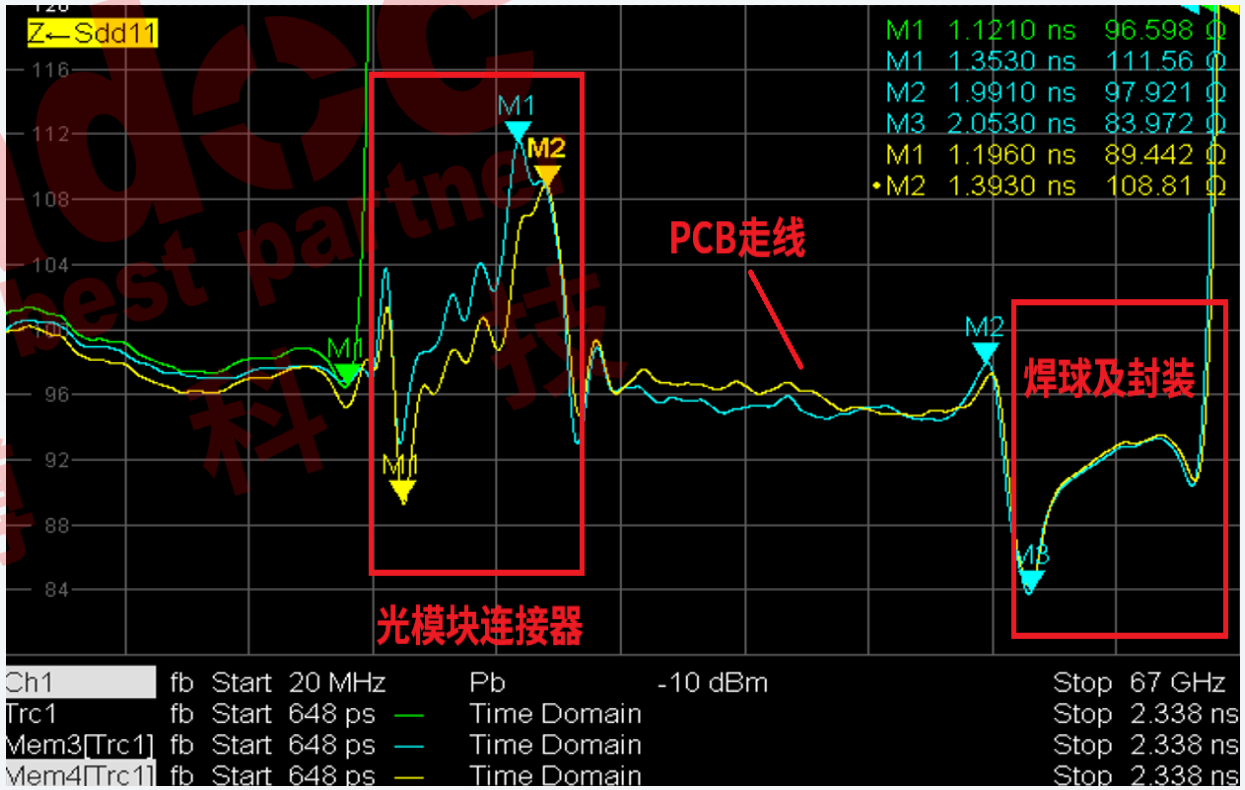


# 第一版加工后的阻抗测试

- 该版本的测试链路示意图及阻抗测试结果如下，从HCB夹具到芯片

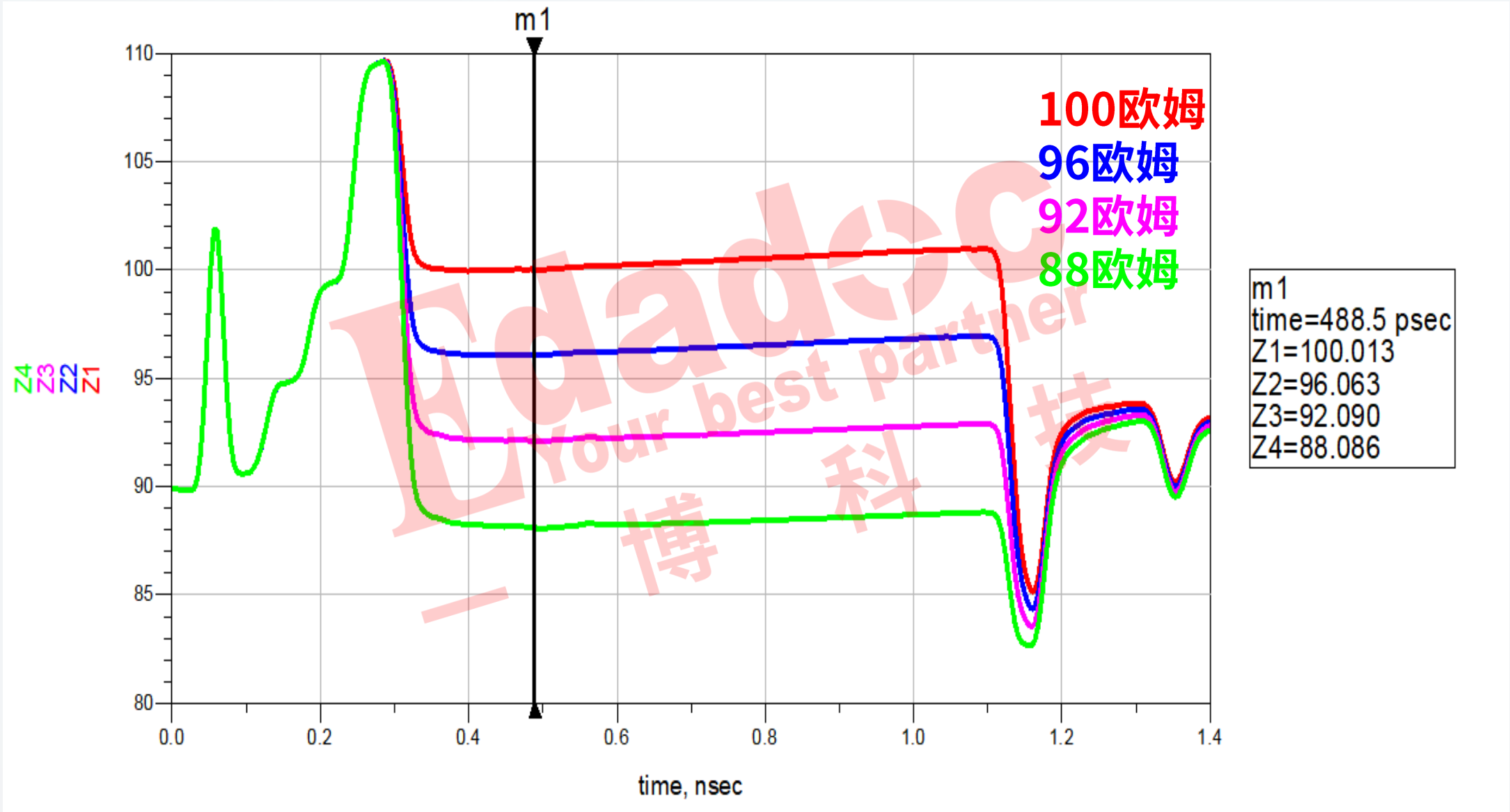




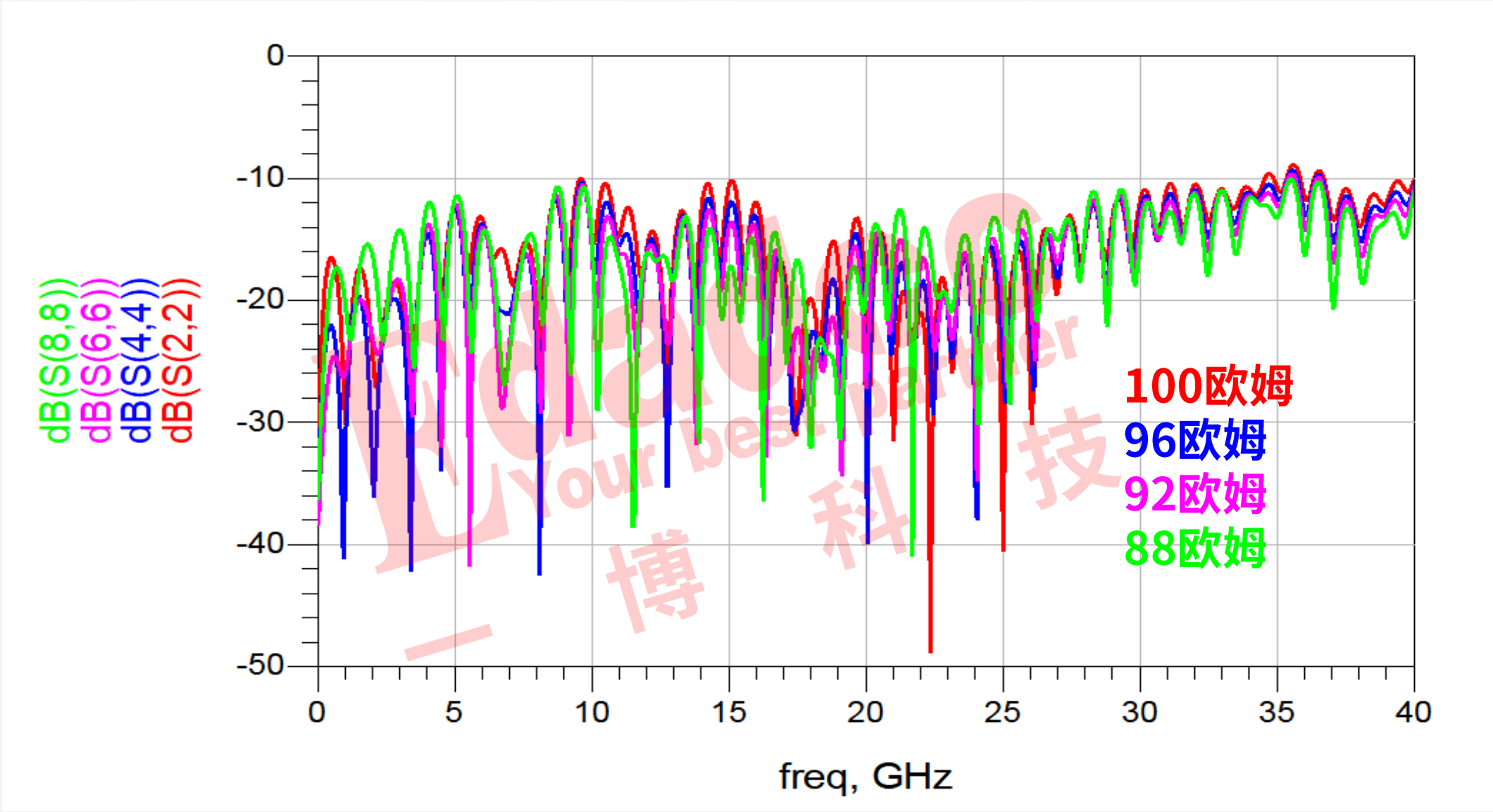
# 建模仿真不同走线阻抗的影响

- 建模仿真不同走线阻抗的影响



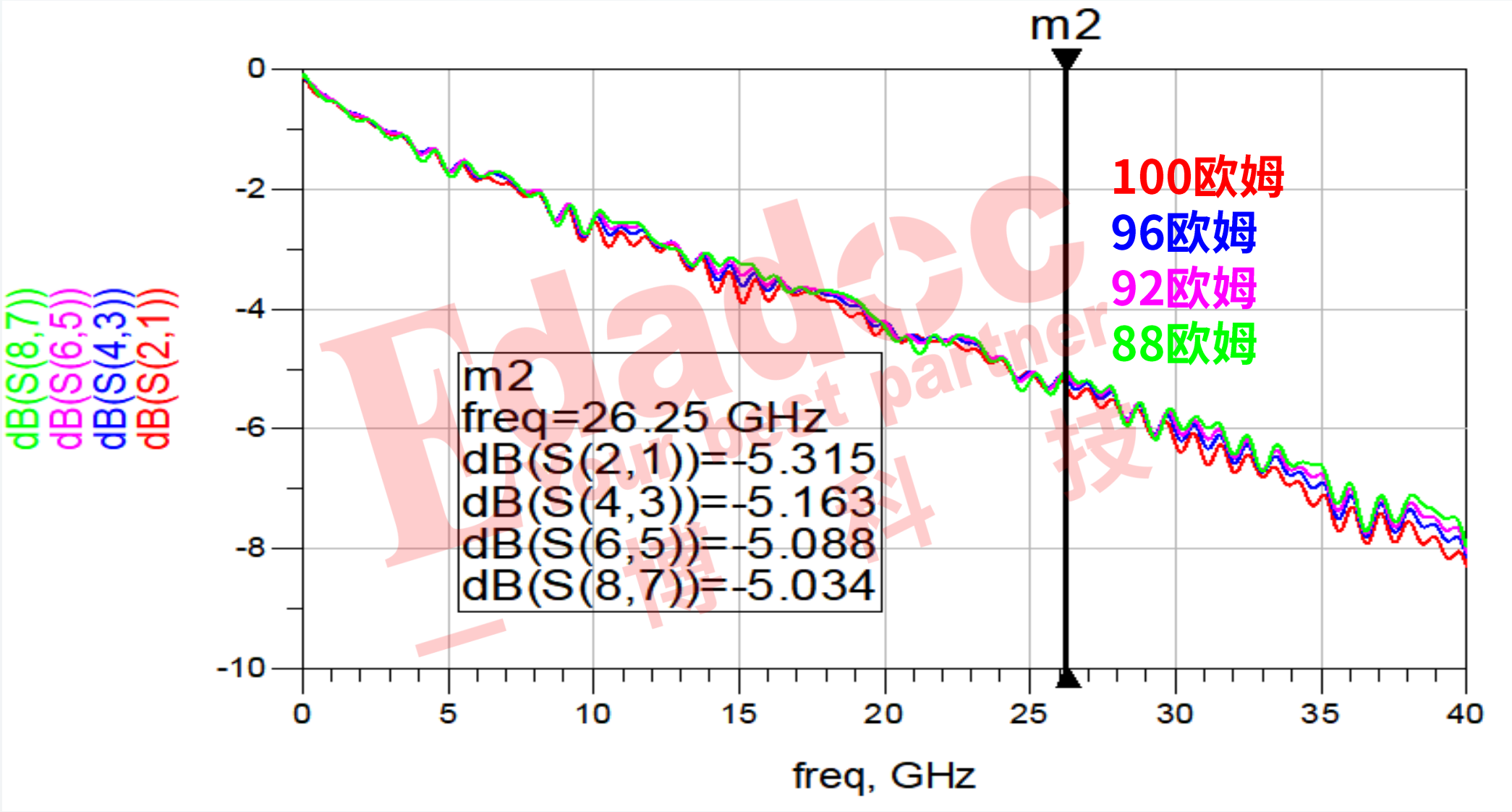
# 建模仿真不同走线阻抗的影响

- 回损仿真对比



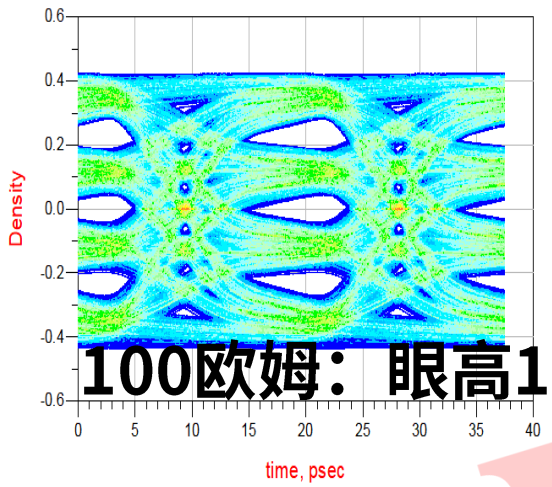
# 建模仿真不同走线阻抗的影响

- 插损仿真对比



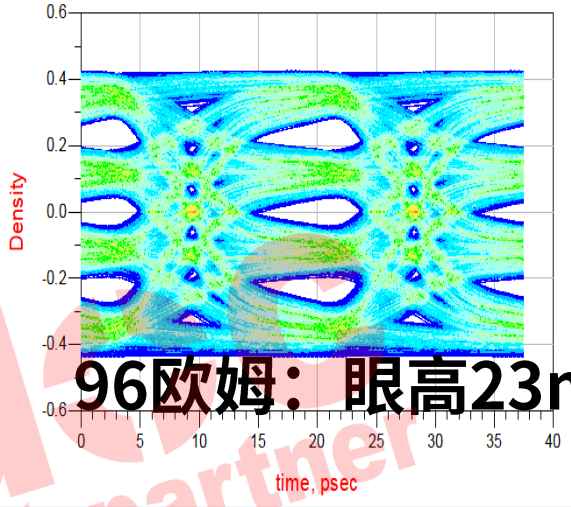
# 建模仿真不同走线阻抗的影响

- 100ohm-96ohm-92ohm-88ohm传输线眼图仿真对比



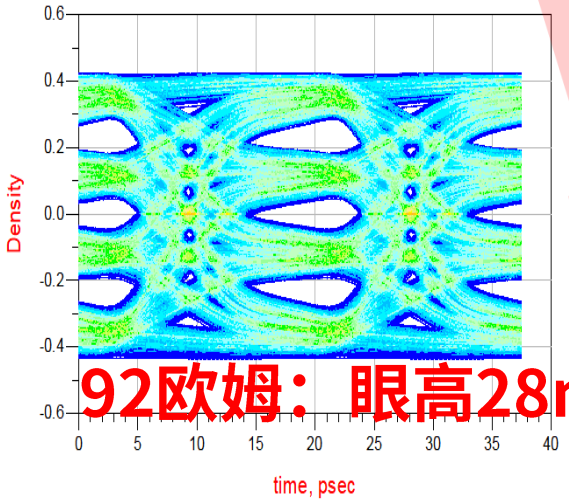

| measurement | Summary |
|---|---|
| WidthAtBER0 | 1.596E-12 |
| WidthAtBER1 | 2.722E-12 |
| WidthAtBER2 | 5.820E-12 |
| HeightAtBER0 | 0.018 |
| HeightAtBER1 | 0.030 |
| HeightAtBER2 | 0.066 |
| Tmid | 1.924E-11 |
| Vlow | -0.589 |
| Vmid | -0.544 |
| Vupp | 0.047 |
| Hlow | 1.877E-13 |
| Hmid | 9.387E-14 |
| Hupp | 5.069E-12 |
| AVlow | 0.231 |
| AVmid | 0.233 |
| AVupp | 0.222 |

**100欧姆：眼高18mV**



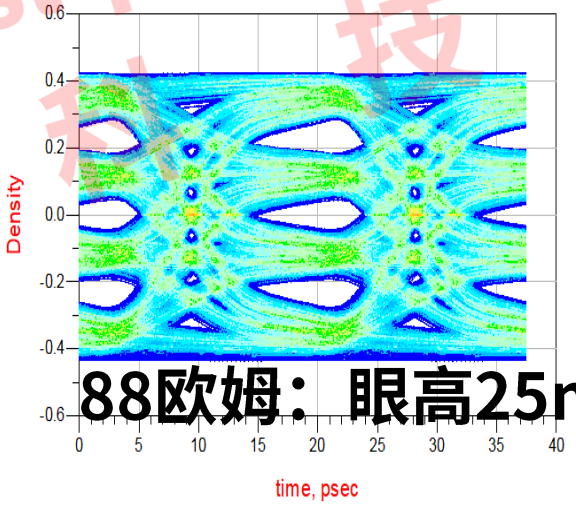

| measurement | Summary |
|---|---|
| WidthAtBER0 | 3.004E-12 |
| WidthAtBER1 | 3.379E-12 |
| WidthAtBER2 | 5.820E-12 |
| HeightAtBER0 | 0.023 |
| HeightAtBER1 | 0.037 |
| HeightAtBER2 | 0.073 |
| Tmid | 1.924E-11 |
| Vlow | 0.014 |
| Vmid | -0.102 |
| Vupp | 0.050 |
| Hlow | 2.910E-12 |
| Hmid | 1.877E-13 |
| Hupp | 5.351E-12 |
| AVlow | 0.232 |
| AVmid | 0.231 |
| AVupp | 0.223 |

**96欧姆：眼高23mV**




| measurement | Summary |
|---|---|
| WidthAtBER0 | 3.755E-12 |
| WidthAtBER1 | 4.694E-12 |
| WidthAtBER2 | 6.477E-12 |
| HeightAtBER0 | 0.028 |
| HeightAtBER1 | 0.043 |
| HeightAtBER2 | 0.079 |
| Tmid | 1.906E-11 |
| Vlow | 0.018 |
| Vmid | 0.017 |
| Vupp | 0.051 |
| Hlow | 3.661E-12 |
| Hmid | 4.224E-12 |
| Hupp | 5.914E-12 |
| AVlow | 0.233 |
| AVmid | 0.231 |
| AVupp | 0.224 |

**92欧姆：眼高28mV**

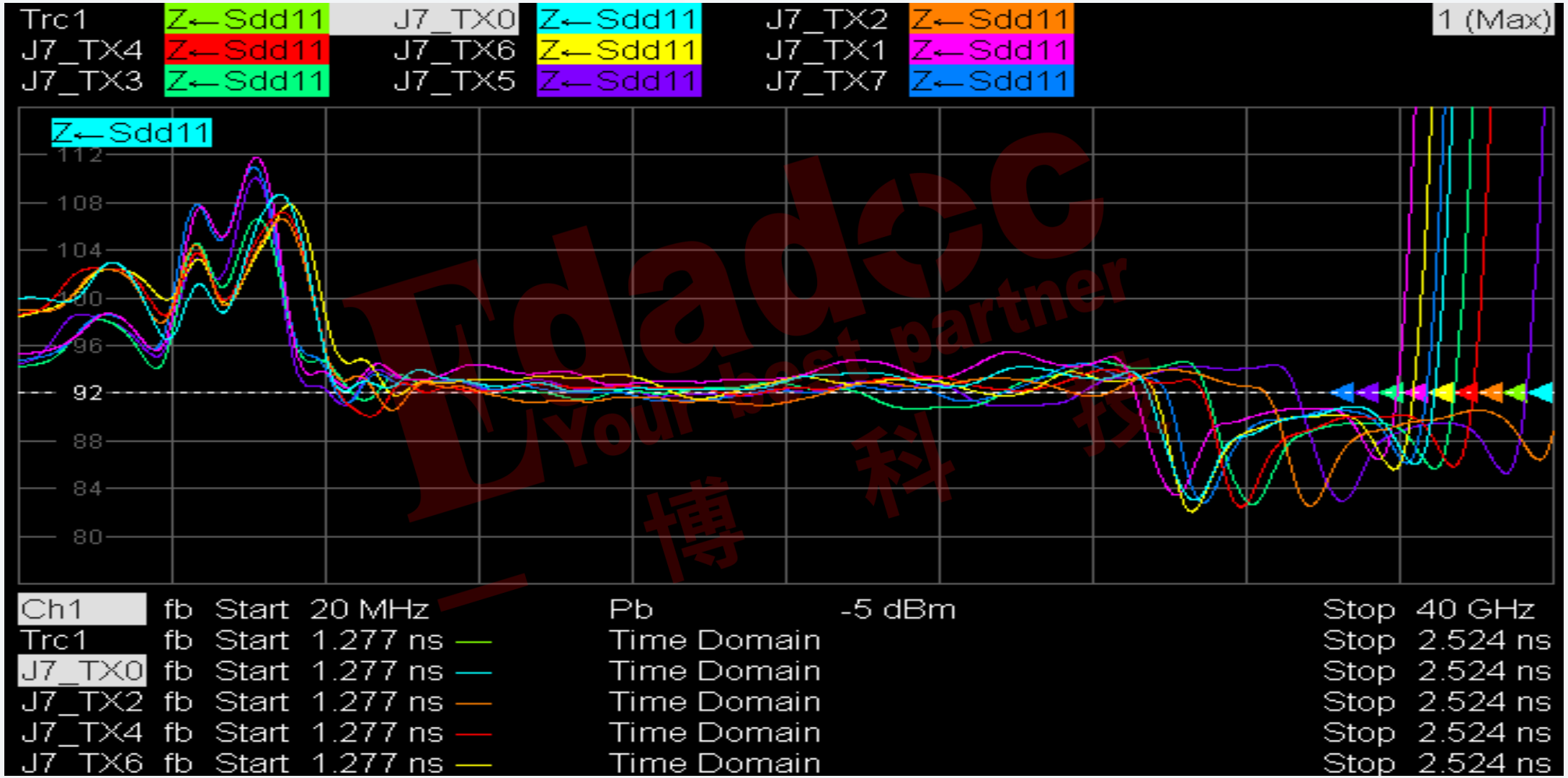



| measurement | Summary |
|---|---|
| WidthAtBER0 | 3.379E-12 |
| WidthAtBER1 | 4.130E-12 |
| WidthAtBER2 | 6.195E-12 |
| HeightAtBER0 | 0.025 |
| HeightAtBER1 | 0.040 |
| HeightAtBER2 | 0.074 |
| Tmid | 1.906E-11 |
| Vlow | 0.016 |
| Vmid | 0.016 |
| Vupp | 0.048 |
| Hlow | 3.098E-12 |
| Hmid | 3.849E-12 |
| Hupp | 5.444E-12 |
| AVlow | 0.232 |
| AVmid | 0.230 |
| AVupp | 0.223 |

**88欧姆：眼高25mV**

# 第二版加工后的阻抗测试

- 走线阻抗控制92欧姆再做一版，误码率测试提升了2个级别，接近1E-9。
- TDR阻抗测试结果如下：



# 结论

1. 传输线阻抗是高速链路的重要影响因素，阻抗的变化对于不同速率的信号会有不同程度的影响；
2. 在大部分速率下（56Gbps及以下），传输线阻抗的设计值选择比起加工误差更影响信号质量；
3. 没必要纠结1欧姆左右的加工误差，测试的值本身也会受到各种外部因素的影响；
4. 112G以上的信号的确需要重视阻抗的设计值和加工误差，这个速率下传输线阻抗的变化对信号质量的影响的确变得很大。

# 一博珠海板厂一期已投产运营

一博珠海PCB板厂


## 一站式硬件创新平台

## PCB设计--制板--元器件--焊接组装

一博旗下控股子公司，珠海全新板厂位于珠海金湾区，占地面积4.5万平方米，年产量180万平米，规划分两期建设，一期全面投产专注于高端快件，提供高品质的高多层、高速、高精密、HDI等PCB生产制造。二期提供中大批量高速、高多层PCB生产。

**珠海板厂距离一博珠海基地17公里、20分钟车程**，实现快速的PCB设计研发到高品质、短交期的PCB及PCBA生产服务。

一博助力客户缩短研发生产周期、聚焦客户痛点及难点，提供PCB设计、制板、焊接加工的一站式解决方案。

# 一博珠海板厂定位

| | | |
|---|---|---|
| 60:1<br>成品孔厚径比 | 120层<br>层数 | ±5%<br>阻抗控制精度 |
| ≤8天<br>10-20层交付周期 | 高端+快件<br>工厂定位 | 0.11mm<br>机械孔钻孔孔径 |
| 40um<br>线宽线间距 | 500+订单/天<br>规划产量规模 | 1-4mil<br>背钻STUB |

聚焦高端AI算力卡（高阶HDI）、高端服务器、ATE（晶圆测试）、工控、汽车电子、高端消费类、医疗、航空航天、网络设备、军工、光模块等产品。致力于推动国内PCB行业的技术进步，尤其是高速、高多层的复杂PCB产品的快速交付，20层及以下制板交期<8天，22层及以上在2周内交付，达到行业领先水平。产品广泛应用于工控、通讯、半导体测试、数据中心、AI算力等领域。

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# THANK YOU!

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